6V, 2A, 1MHz, CMCOT Synchronous Step-Down Converter

General Description

The RT8097A is a simple, easy-to-use, 2A synchronous step-down DC-DC converter with an input supply voltage range of 2.7V to 6V. The device build-in an accurate 0.6V (typ.) reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in a SOT-23-5 and SOT-23-6 packages.

The RT8097A adopts Current Mode Constant On-Time (CMCOT) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT8097A operates in automatic PSM that maintains high efficiency during light load operation.

The RT8097A senses low-side FETs current for a robust over-current protection. It features cycle-by-cycle current limit protection and prevent the device from the catastrophic damage in output short circuit, over current or inductor saturation. An internally adjustable soft-start function prevents inrush current during start-up. The device also includes input under-voltage lockout, output under-voltage protection, and over-temperature protection (thermal shutdown) to provide safe and smooth operation in all operating conditions. The RT8097A is offered in a SOT-23-5 and SOT-23-6 packages.

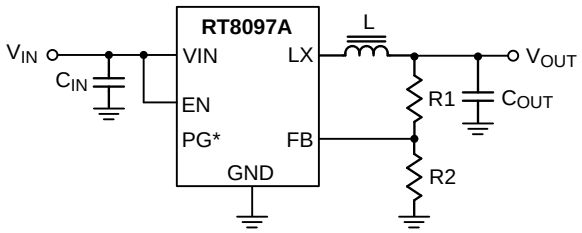
Features

- **Efficiency Up to 95%**
- **2A Converter With Built-In 100mΩ/70mΩ Low $R_{DS(ON)}$ Power FETs**
- **Input Supply Voltage Range : 2.7V to 6V**
- **Output Voltage Range : 0.6V to 3.4V**
- **Current Mode Constant On-Time (CMCOT) Control**
- **Ultrafast Transient Response**
- **No Needs For External Compensations**
- **Optimized for Low-ESR Ceramic Output Capacitors**
- **0.6V ±1.5% High-Accuracy Feedback Reference Voltage**
- **LS FETs Protection for Robust Over-Current Protection**
- **Power Saving in Light Load**
- **Fixed Switching Frequency : 1MHz (typ.)**
- **Internally Soft-Start Function**
- **Monotonic Start-Up for Pre-Biased Output**
- **Input Under-Voltage Lockout (UVLO)**
- **Output Under-Voltage Protection (UVP) with Hiccup Mode**
- **Power Good Indication in SOT-23-6 Package**
- **Enable Control**
- **Available In SOT-23-5 and SOT-23-6 Packages**

Applications

- STB, Cable Modem, & xDSL Platforms
- LCD TV Power Supply & Metering Platforms
- General Purpose Point of Load (POL)

Simplified Application Circuit



*For SOT-23-6 Package Only

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Ordering Information

RT8097A□□□

- Package Type
  - B : SOT-23-5
  - E : SOT-23-6
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- UVP Option
  - H : Hiccup
  - L : Latched-Off
- A : PSM/PWM

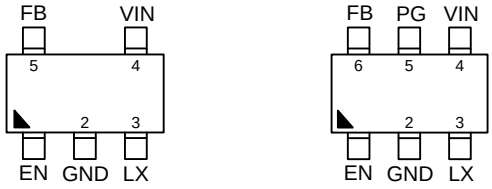
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



SOT-23-5 SOT-23-6

Marking Information

RT8097AHGB

4N=DNN

4N= : Product Code
DNN : Date Code

RT8097ALGB

4M=DNN

4M= : Product Code
DNN : Date Code

RT8097AHGE

1V=DNN

1V= : Product Code
DNN : Date Code

RT8097ALGE

1U=DNN

1U= : Product Code
DNN : Date Code

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOT-23-5	SOT-23-6		
1	1	EN	Enable control input.
2	2	GND	Power ground.
3	3	LX	Switch node.
4	4	VIN	Supply voltage input. The RT8097A operates from a 2.7V to 6V input.
5	6	FB	Feedback voltage input. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
--	5	PG	Power good indicator. The output of this pin is an open-drain with external pull-up resistor. PG is pulled up when the FB voltage is within 90% (typ.) otherwise it is LOW.

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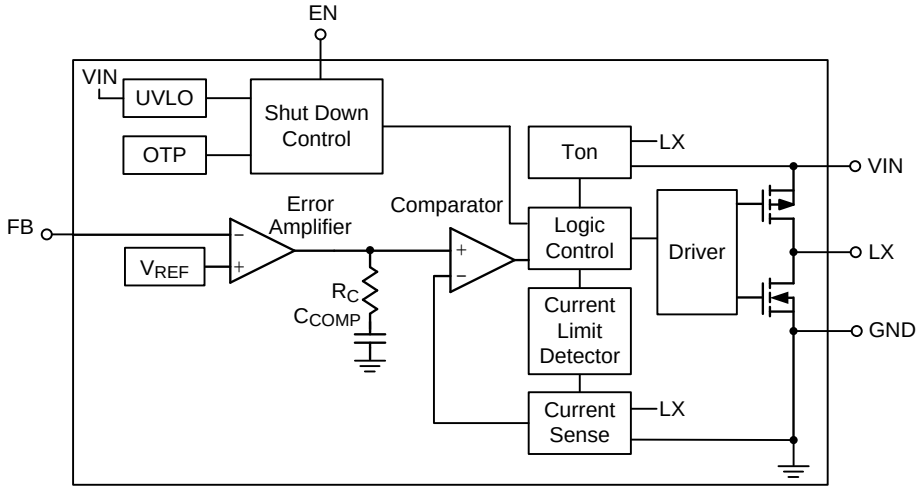
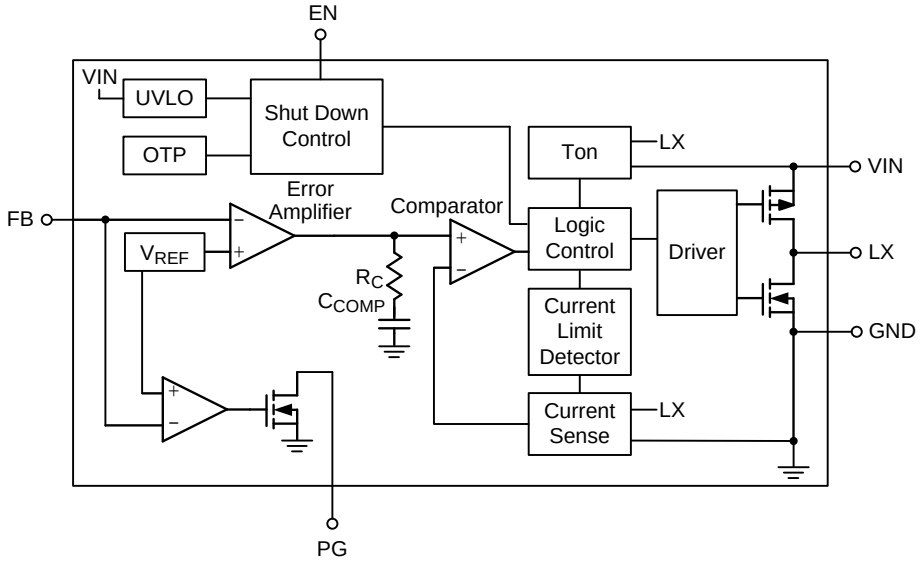
Functional Block Diagram

For SOT-23-5 Package



For SOT-23-6 Package



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Operation

The RT8097A is a synchronous low voltage step-down converter that can support the input voltage range from 2.7V to 6V and the output current can be up to 2A. The RT8097A uses a constant on-time, current mode architecture. In normal operation, the high side P-MOSFET is turned on when the switch controller is set by the comparator and is turned off when the Ton comparator resets the switch controller.

Low side MOSFET peak current is measured by internal RSENSE. The error amplifier EA adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.6V (typ.) reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

UV Comparator

If the feedback voltage (V_{FB}) is lower than threshold voltage 0.2V (typ.), the UV comparator's output will go high and the switch controller will turn off the high side MOSFET. The output under voltage protection is designed to operate in Hiccup mode for RT8097AH, Latch mode for RT8097AL.

PGOOD Comparator

When the feedback voltage (V_{FB}) is higher than threshold voltage 0.54V (typ.), the PGOOD open drain output will be high impedance. The internal PG MOSFET is typical 10Ω. The PGOOD signal delay time from EN is about 2ms (typ.).

Enable Comparator

A logic-high enables the converter; a logic-low forces the IC into shutdown mode.

Soft-Start (SS)

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 1.2ms.

Over Current Protection (OCP)

The RT8097A provides over current protection by detecting low side MOSFET valley inductor current. If the sensed valley inductor current is over the current limit threshold (3.1A typ.), the OCP will be triggered. When OCP is tripped, the RT8097A will keep the over current threshold level then cause the UV protection.

Thermal Shutdown (OTP)

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C (typ.). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature decreases below the hysteresis of 20°C (typ.), the device reinstates the power up sequence.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 6.5V
- LX Pin Switch Voltage ---------- –0.3V to (V_{IN} + 0.3V)
  <20ns ---------- –4.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-5 ---------- 1.02W
  SOT-23-6 ---------- 1.09W
- Package Thermal Resistance (Note 2)
  SOT-23-5, θ_{JA} ---------- 97.8°C/W
  SOT-23-6, θ_{JA} ---------- 91.5°C/W
  SOT-23-5, θ_{JC} ---------- 7.1°C/W
  SOT-23-6, θ_{JC} ---------- 14°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.7V to 6V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		2.7	--	6	V
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
Feedback Leakage Current	I_{FB}	V_{FB} = 3.3V	--	--	1	μA
DC Bias Current		Active ,V_{FB} = 0.63V, not switching	--	22	--	μA
		Shutdown	--	--	1	
Switching Leakage Current			--	--	1	μA
Switching Frequency			0.8	1	1.2	MHz
Switch On Resistance, Low	R_{NMOS}	I_{SW} = 0.3A	--	70	--	mΩ
Switch On Resistance, High	R_{PMOS}	I_{SW} = 0.3A	--	100	--	mΩ
Valley Current Limit	I_{LIM}		2.2	3.1	3.9	A
Under-Voltage Lockout Threshold	V_{UVLO}	VDD rising	--	2.25	2.5	V
		VDD falling	--	2	--	V

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Temperature Threshold				--	150	--	°C
Enable Input Voltage	Logic-High	V_{IH}		1.5	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
PG Pin Threshold (relative to V_{OUT})			Rising	--	90	--	%
			Falling	--	85	--	
PG Open-Drain Impedance (PG = low)				--	10	--	Ω
Soft-Start Time		t_{SS}		--	1.2	--	ms
Minimum Off Time				70	120	180	ns
Output Discharge Switch On Resistance				--	1.8	--	kΩ

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. The first layer of copper area is filled. θ_{JC} is measured at the lead of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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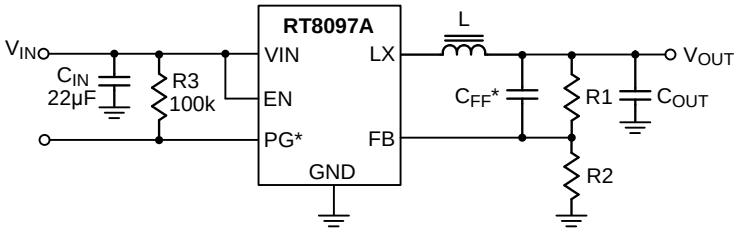
Typical Application Circuit



*For SOT-23-6 Package Only

*C_{FF} : Optional for performance fine-tune

Table 1. Suggested Component Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{IN} (μF)	L (μH)	C_{OUT} (μF)
3.3	90	20	22	1.5	22
1.8	100	50	22	1.5	22
1.5	100	66.6	22	1.5	22
1.2	100	100	22	1.5	22
1.05	100	133	22	1.5	22
1	100	148	22	1.5	22

Note : All input and output capacitance in the suggested parameter mean the effective capacitance. The effective capacitance needs to consider any De-rating effect like DC bias.

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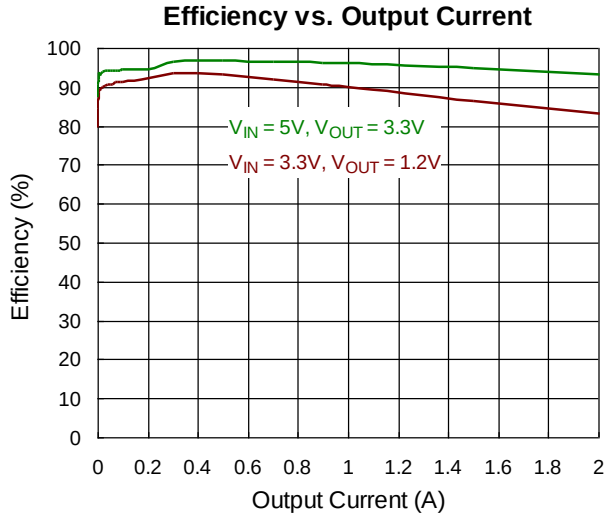
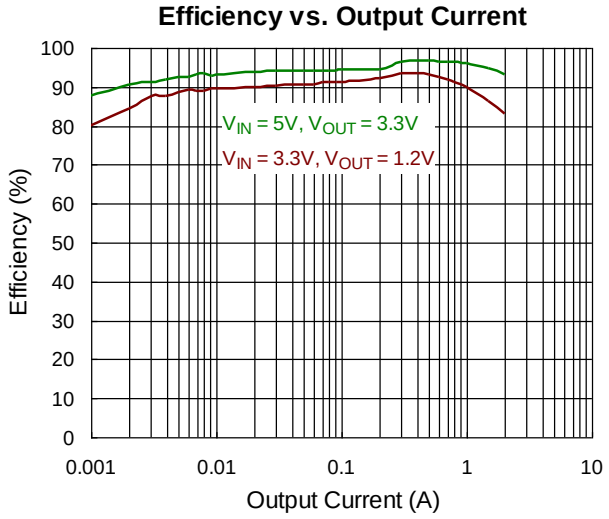
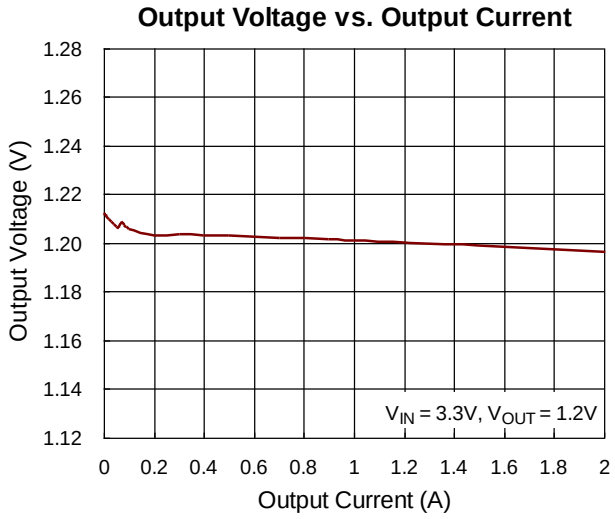
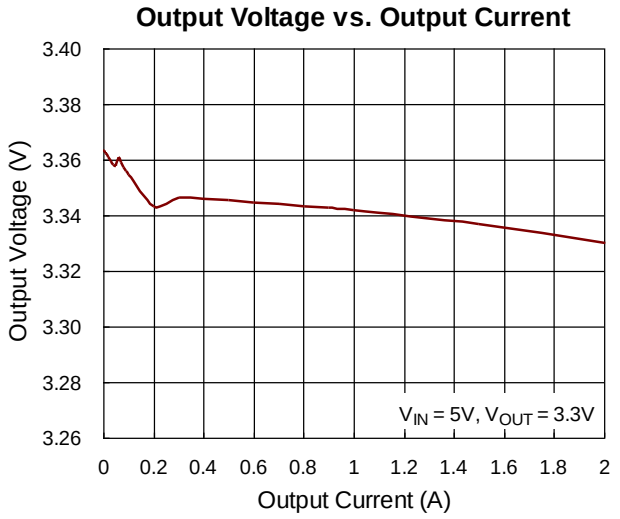
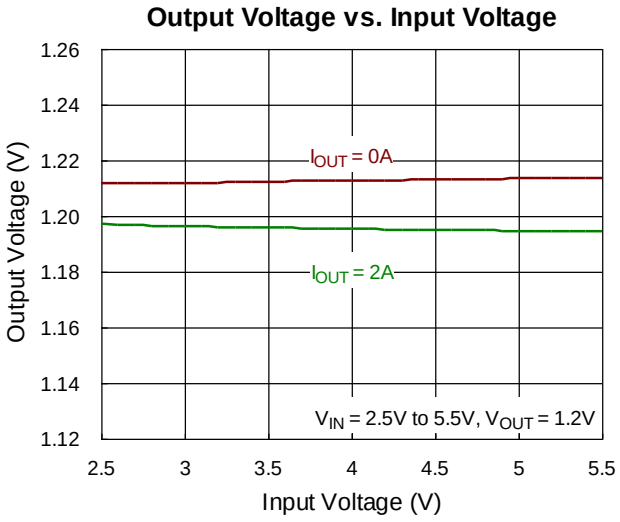
Typical Operating Characteristics

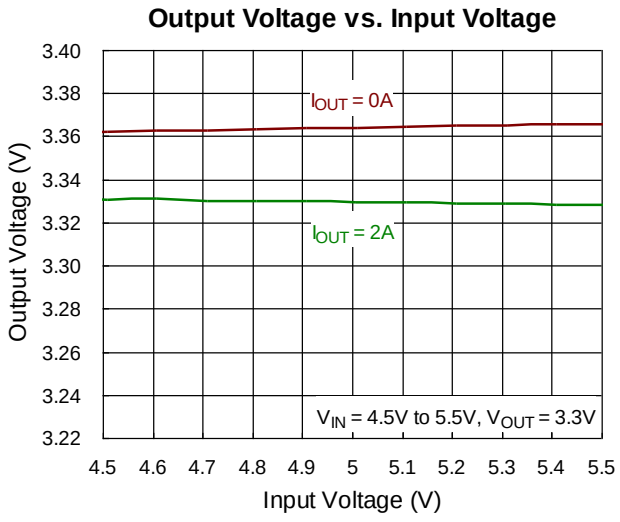












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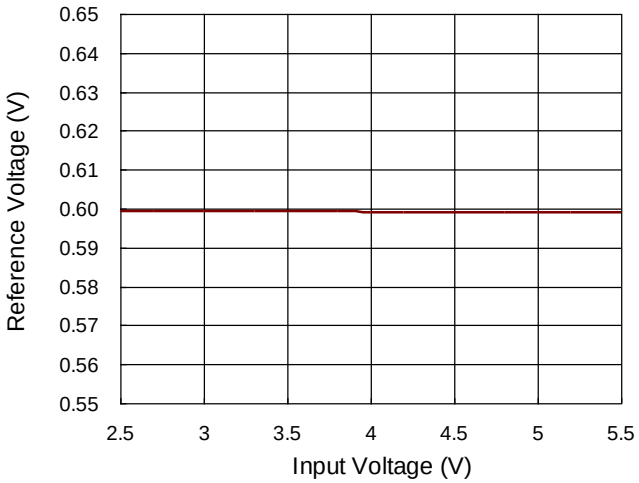
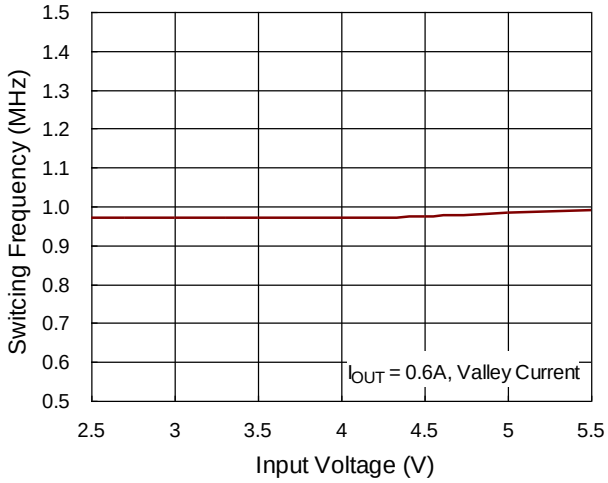
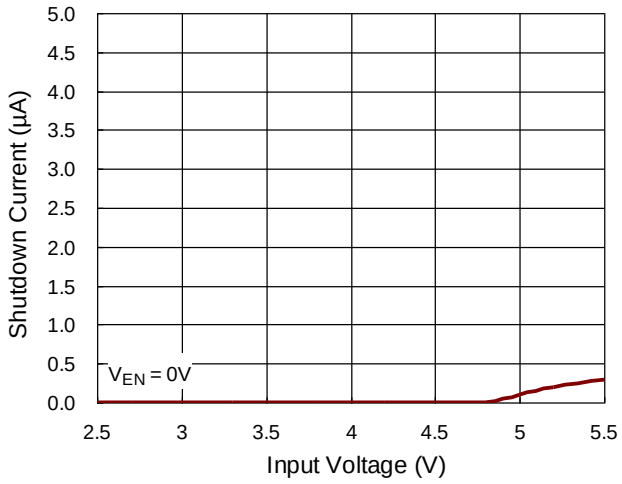
Reference Voltage vs. Input Voltage



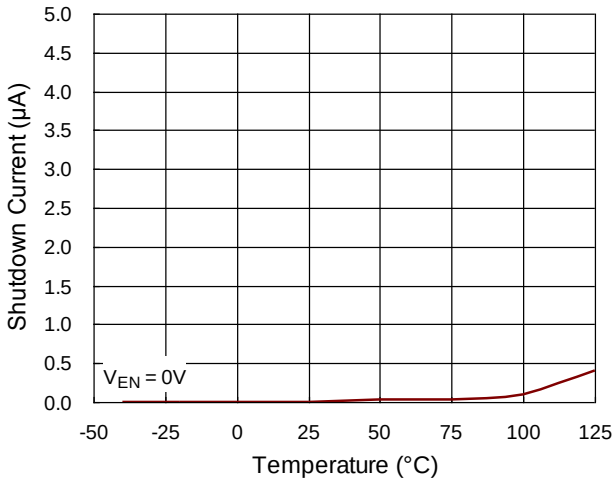
Switching Frequency vs. Input Voltage



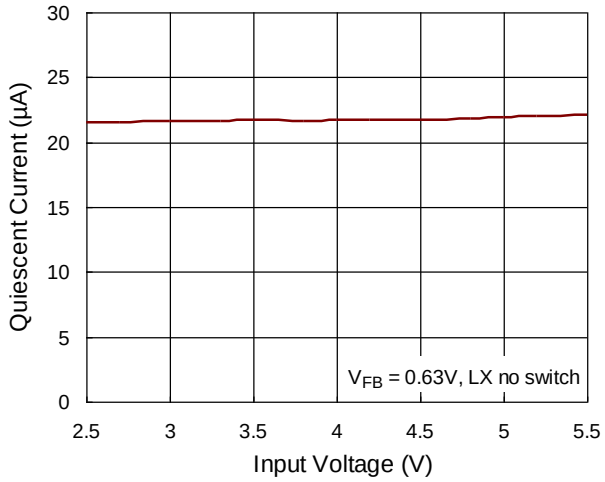
Shutdown Current vs. Input Voltage



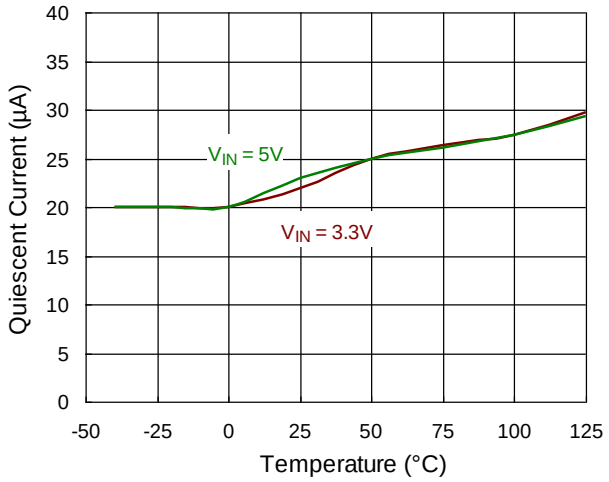
Shutdown Currrent vs. Temperature



Quiescent Current vs. Input Voltage



Quiescent Current vs. Temperature



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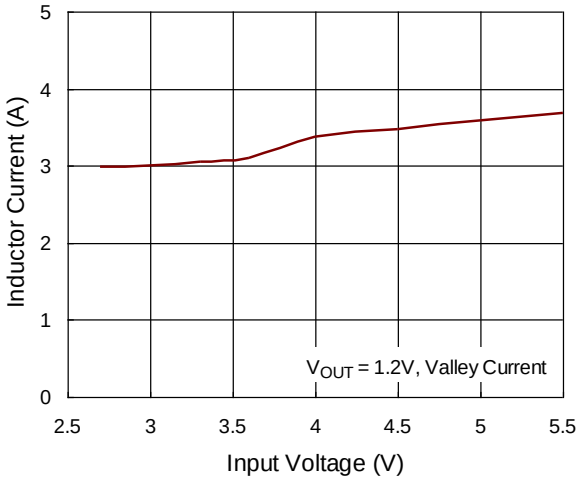
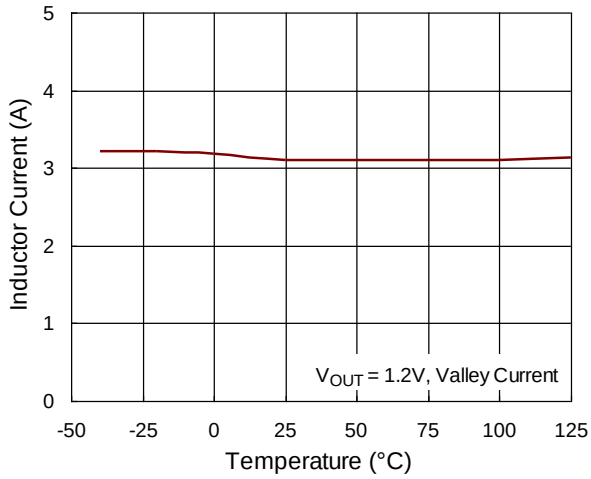
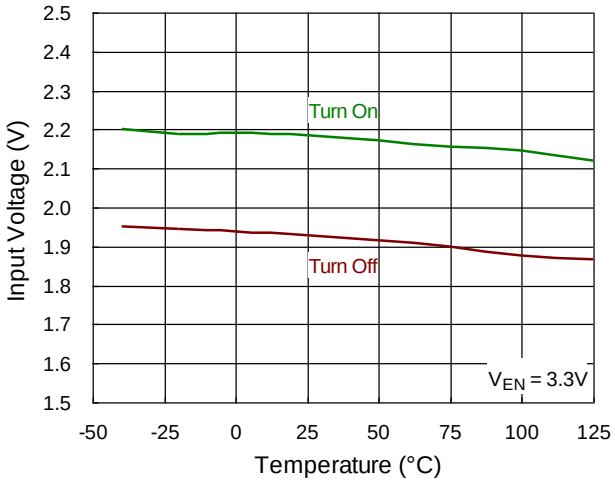
Inductor Current Limit vs. Input Voltage



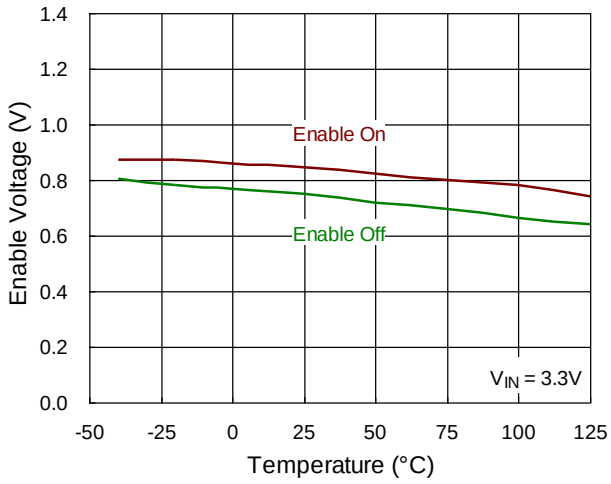
Inductor Current Limit vs. Temperature



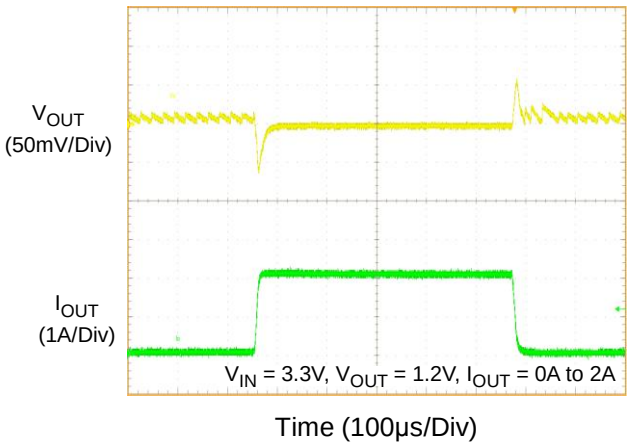
UVLO vs. Temperature



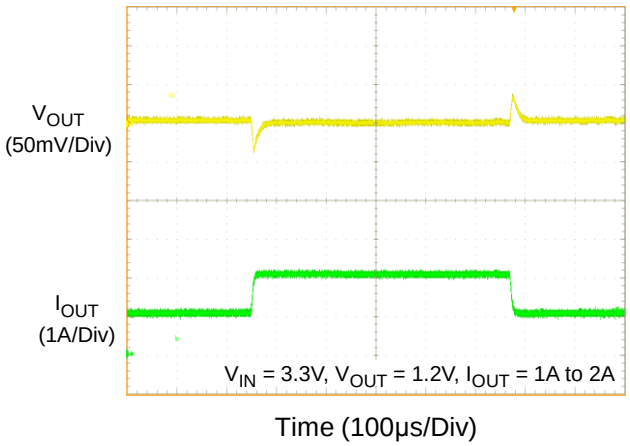
Enable Voltage vs. Temperature



Load Transient Response



Load Transient Response



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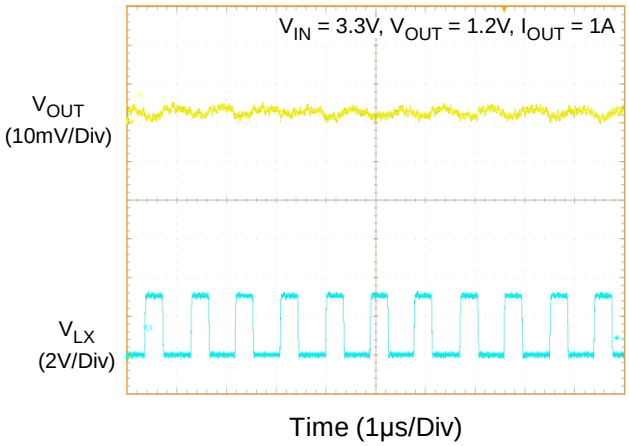
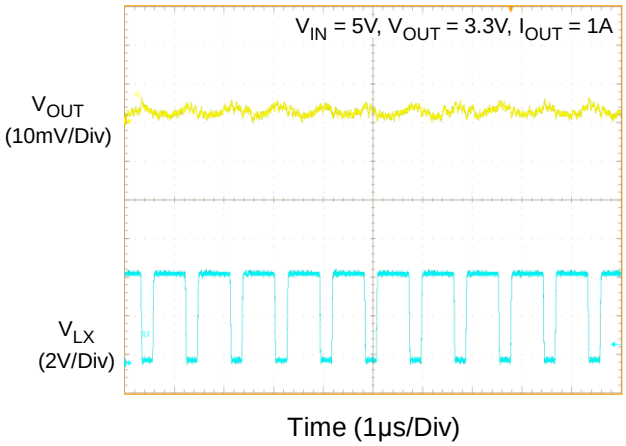
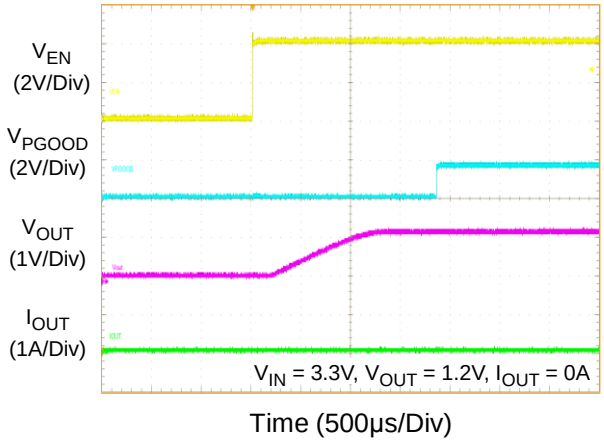
Voltage Ripple



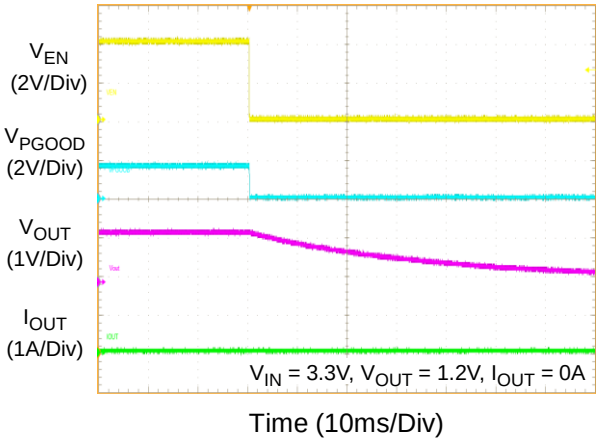
Voltage Ripple



Power On from EN



Power Off from EN



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Application Information

The RT8097A is a single-phase step-down converter. It provides single feedback loop constant on-time, current mode control with fast transient response. An internal 0.6V (typ.) reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1MHz, typ.) oscillator and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.6V (typ.).

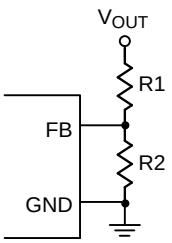

Figure 1. Setting V_{OUT} with a Voltage Divider

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8097A remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the V_{EN} trip point, the RT8097A begins a new initialization and soft-start cycle.

Internal Soft-Start

The RT8097A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the input surge current. The internal 0.6V (typ.) reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V (typ.).

Over Voltage Protection (OVP)

The RT8097AL provide Over Voltage Protection function when output voltage over (120%, typ.). The IC will be into Latch-off mode.

UVLO Protection

The RT8097A has input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.25V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with equivalent capacitance greater than 22μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{IN_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. One good design uses more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

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The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (V_{P-P}) can be calculated by the following equation :

$$V_{P_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag and soar during load transient. The voltage sag (V_{SAG}) and soar (V_{SOAR}) can be calculated by the following equation :

$$V_{SAG} = V_{SOAR} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag and soar specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag and soar is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag and soar. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor.

Inductor saturation current should be chosen over IC's current limit.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT-23-5 package, the thermal resistance, θ_{JA}, is 97.8°C/W on a standard four-layer thermal test board. For SOT-23-6 package, the thermal resistance, θ_{JA}, is 91.5°C/W on a standard four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (97.8 °C/W) = 1.02W for SOT-23-5 package

$P_{D(MAX)}$ = (125°C − 25°C) / (91.5°C/W) = 1.09W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

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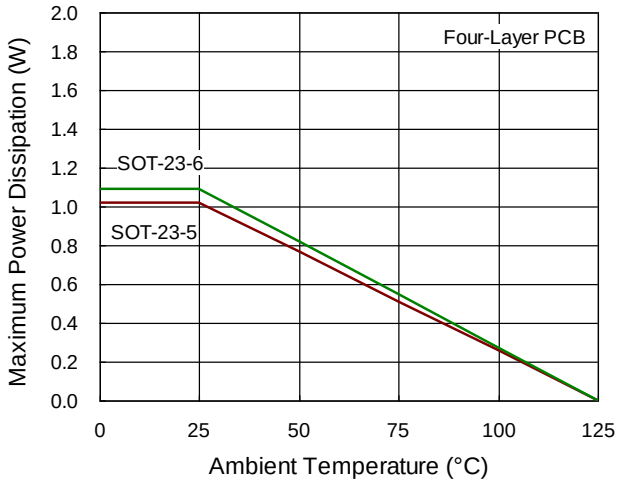

Figure 2. Derating Curve of Maximum Power Dissipation

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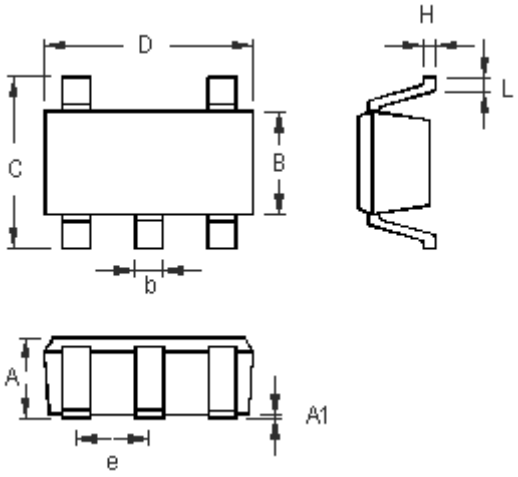
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

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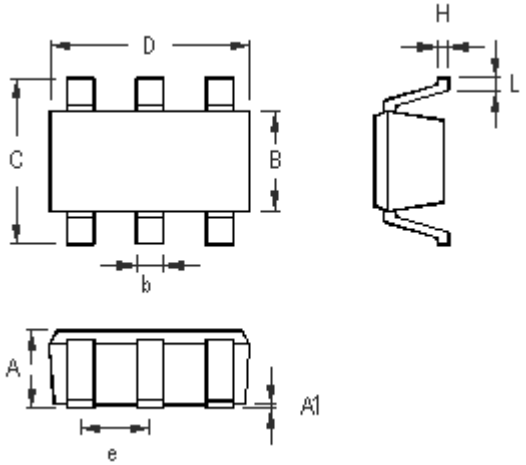

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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