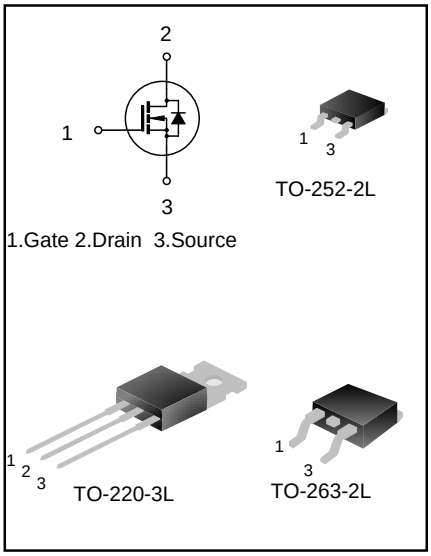
120A, 80V N-CHANNEL MOSFET

DESCRIPTION

SVG086R0NT(S)(D) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in UPS, Power Management for Inverter Systems.



FEATURES

- 120A, 80V, $R_{DS(on)(typ.)}$=5.0mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVG086R0NT	TO-220-3L	086R0NT	Pb free	Tube
SVG086R0NS	TO-263-2L	086R0NS	Pb free	Tube
SVG086R0NSTR	TO-263-2L	086R0NS	Pb free	Tape&Reel
SVG086R0NDTR	TO-252-2L	086R0ND	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, T_C=25°C)

Characteristics		Symbol	Ratings		Unit
			SVG086R0NT/NS	SVG086R0ND	
Drain-Source Voltage		V_{DS}	80		V
Gate-Source Voltage		V_{GS}	±20		V
Drain Current	T_C=25°C	I_D	120		A
	T_C=100°C		76		
Drain Current Pulsed		I_{DM}	480		A
Power Dissipation(T_C=25°C)		P_D	156	114	W
-Derate above 25°C			1.3	0.9	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	306		mJ
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVG086R0NT/NS	SVG086R0ND	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.8	1.1	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_C=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	80	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=50A	--	5.0	6.0	mΩ
Gate Resistance	R_G	f=1MHz	--	2.2	--	Ω
Input Capacitance	C_{iss}	f=1MHz,V_{GS}=0V,V_{DS}=40V	--	3896	--	pF
Output Capacitance	C_{oss}		--	520	--	
Reverse Transfer Capacitance	C_{rss}		--	25	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=40V, V_{GS}=10V, R_G=3.5Ω, I_D=10A (Note 2,3)	--	22	--	ns
Turn-on Rise Time	t_r		--	35	--	
Turn-off Delay Time	$t_{d(off)}$		--	56	--	
Turn-off Fall Time	t_f		--	19	--	
Total Gate Charge	Q_g	V_{DD}=64V, V_{GS}=10V, I_D=50A (Note 2,3)	--	66	--	nC
Gate-Source Charge	Q_{gs}		--	25	--	
Gate-Drain Charge	Q_{gd}		--	17	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	120	A
Pulsed Source Current	I_{SM}		--	--	480	
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=30A,V_{GS}=0V, dIF/dt=100A/μs (Note 2)	--	47	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.06	--	μC

Notes:

1.L=0.5mH, I_{AS}=35A, V_{DD}=50V, R_G=25Ω,starting T_J=25°C;

2.Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;

3.Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

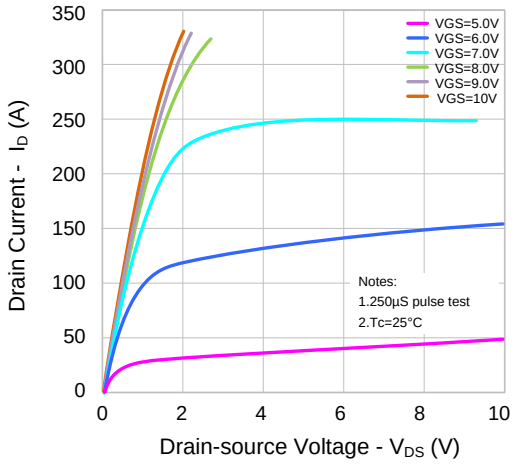


Figure 2. Transfer Characteristics

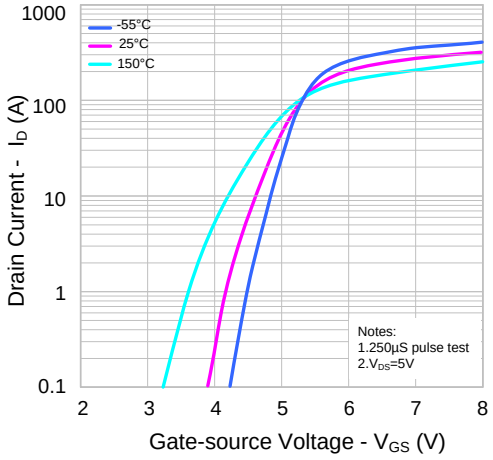


Figure 3. On-resistance vs. Drain Current

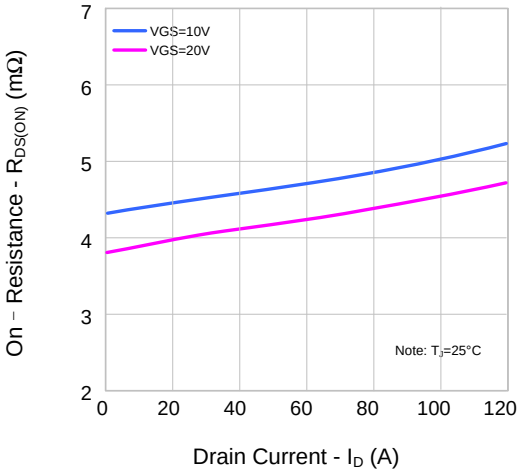


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

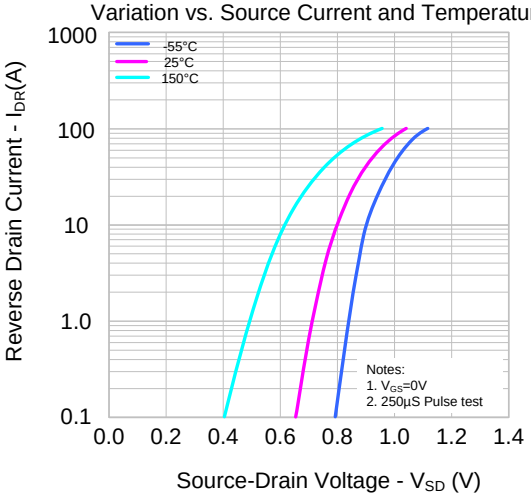


Figure 5. Capacitance Characteristics

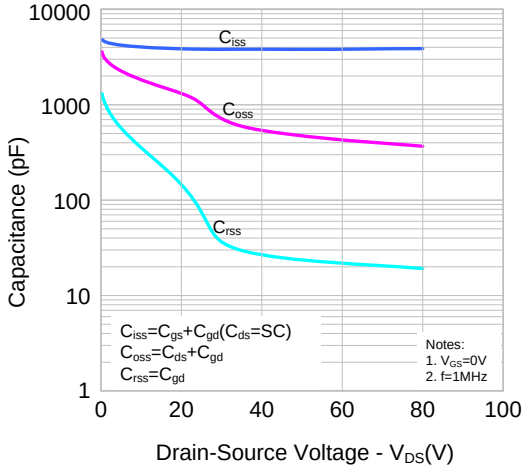
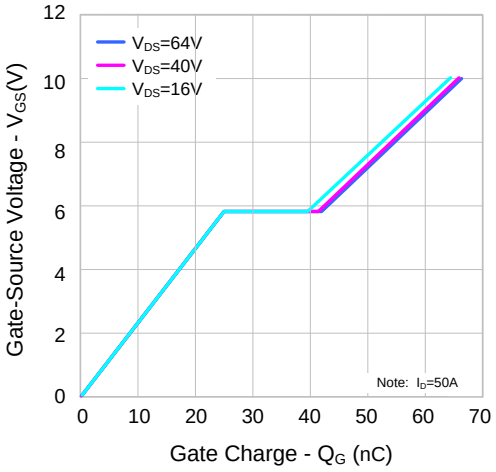


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage vs. Temperature Characteristics

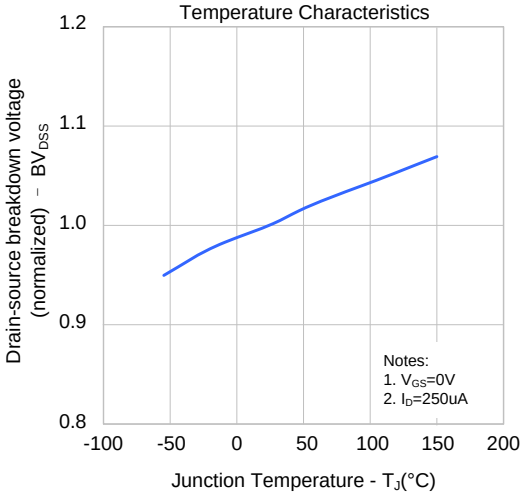


Figure 8. On-resistance vs. Temperature Characteristics

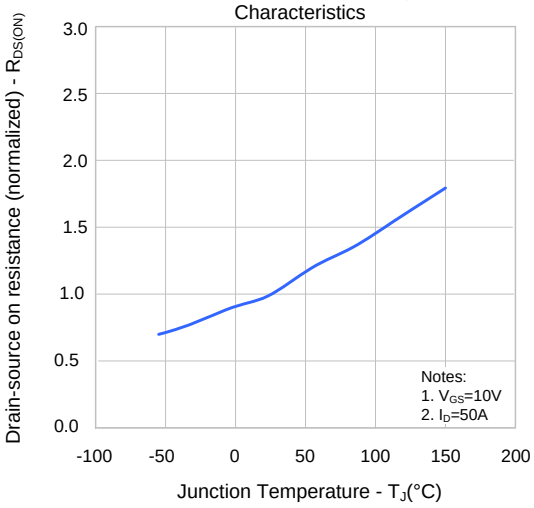


Figure 9-1. Max. Safe Operating Area(SVG086R0NT/NS)

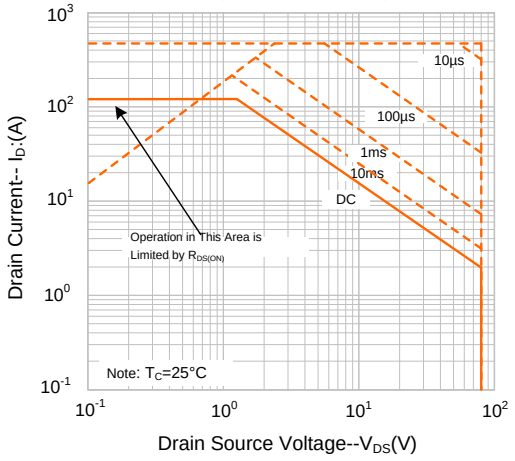
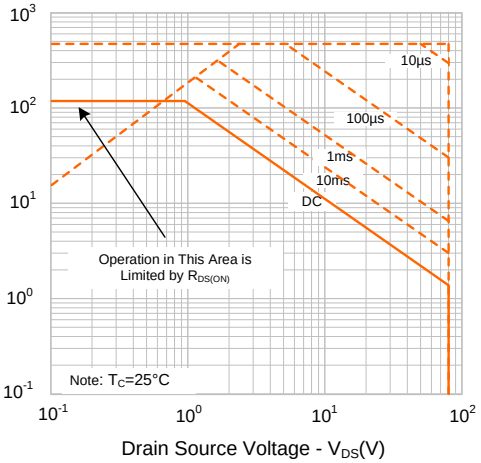
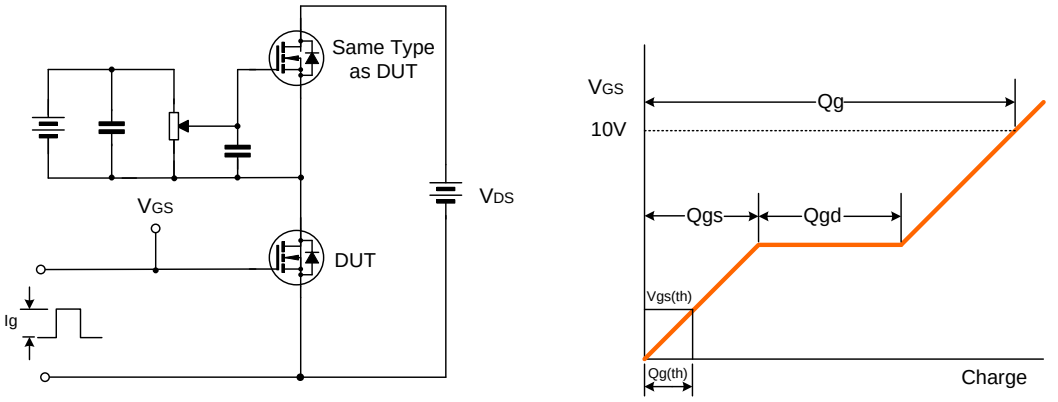


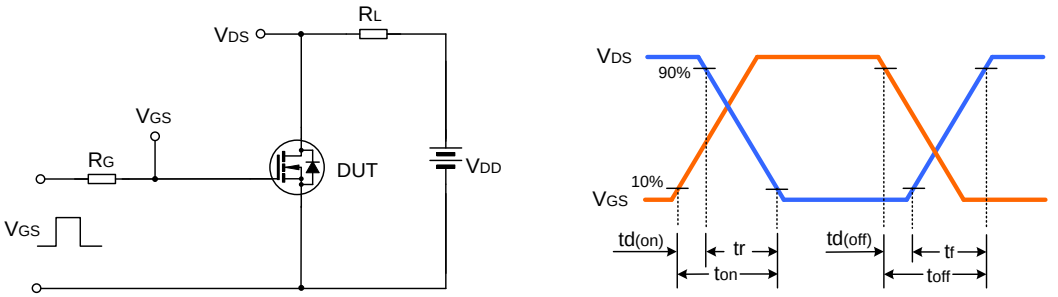
Figure 9-2. Max. Safe Operating Area (SVG086R0ND)



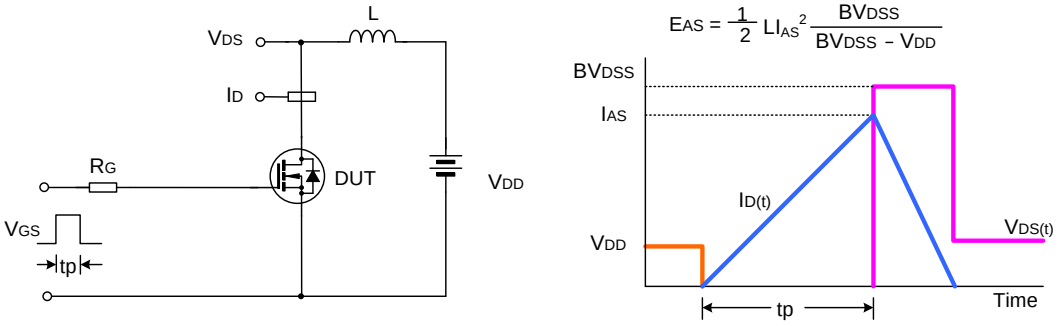
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

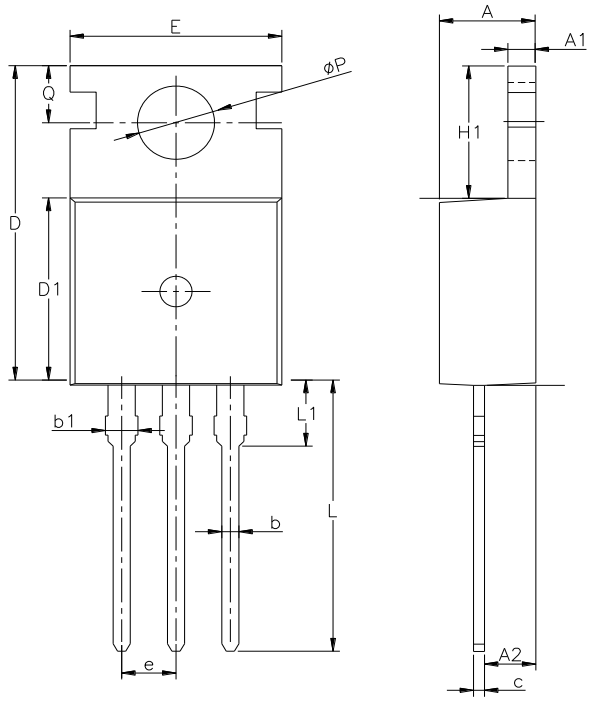


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-220-3L

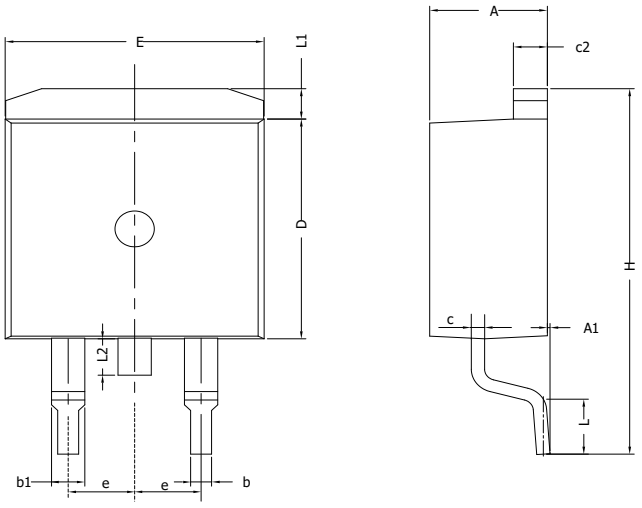
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e		2.54BSC	
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ΦP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-263-2L

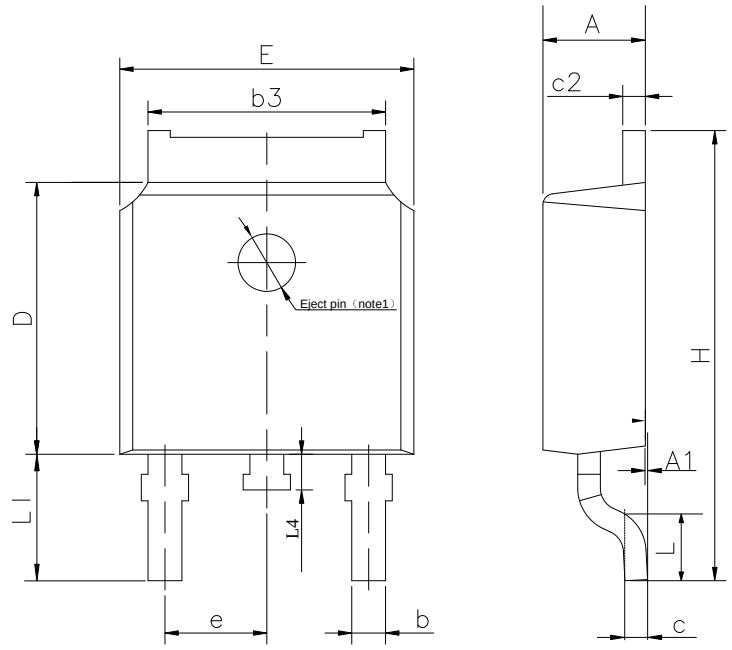
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e		2.54BSC	
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

PACKAGE OUTLINE

TO-252-2L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

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Rev.: 1.3

Revision History:

1. Update Electrical schematic and typical test circuit

Rev.: 1.2

Revision History:

1. Add TO-252-2L

Rev.: 1.1

Revision History:

1. Add TO-263-2L

Rev.: 1.0

Revision History:

1. First release