I²C High-efficiency Bidirectional Buck-Boost Charge-Discharge Controller

1. Description

SW7201 is a high-efficiency synchronous 4-transistor bidirectional buck-boost charge-discharge controller that supports the charge-discharge management of 1-4 cells. It can provide up to 100W output power and support multiple input and output detection and path drive. It can form a simple and complete bidirectional fast charging solution with an MCU and a protocol chip.

2. Applications

- Power Banks
- Power Tools
- Industrial Equipment
- Equipment with Rechargeable Batteries

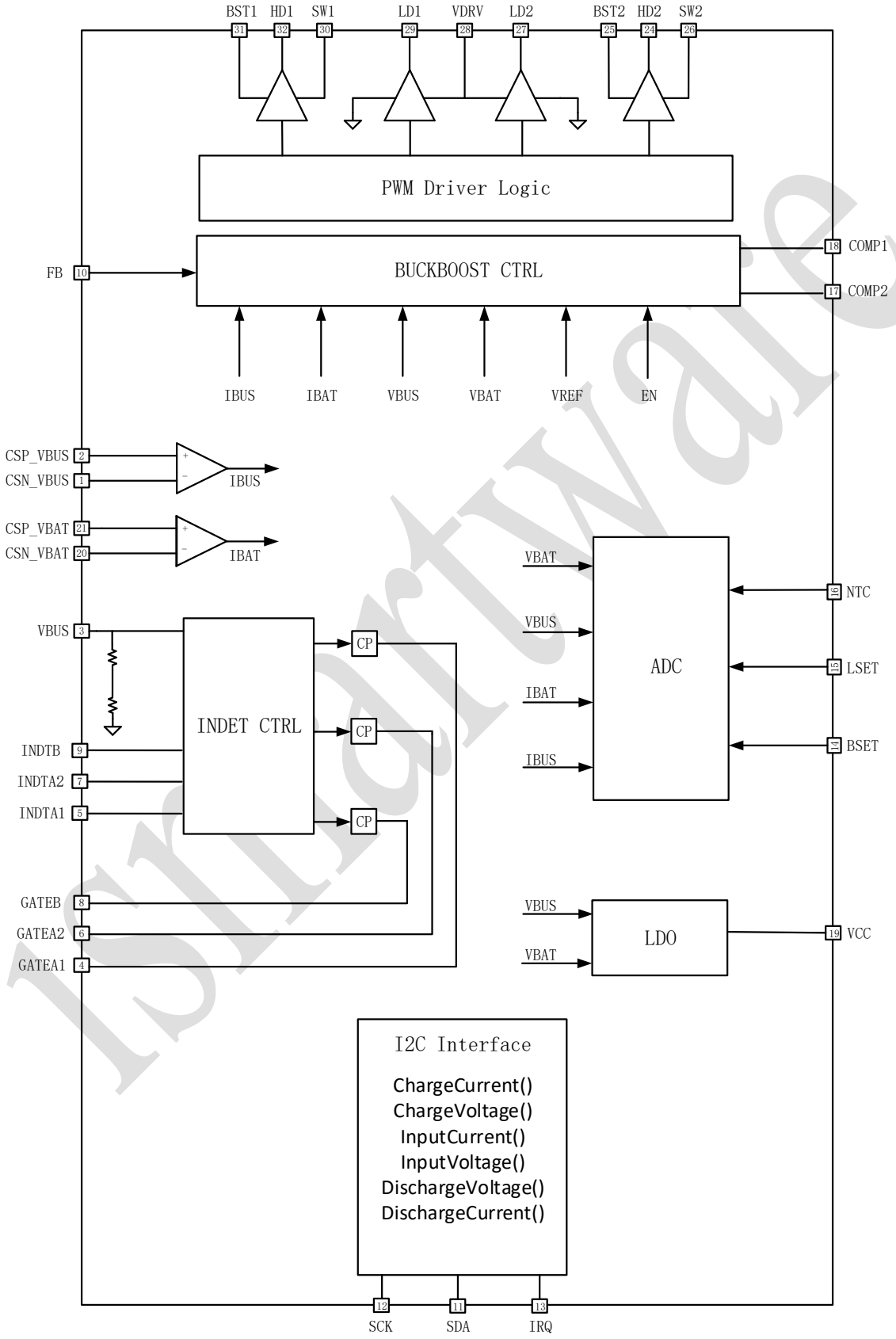
3. Features

- **High-efficiency Buck-boost Charger**
  - Support buck-boost charging of 1 to 4 cells battery
  - Support 3V-19.2V charging target voltage setting
  - Support 100W input power
  - Support 4V-24V input voltage
  - Support I2C programming to control input/battery current limit
  - Seamless switching between boost and buck
- **Reverse Buck-boost Discharge**
  - Support 100W output power
  - Support 3V-22V output voltage
  - Flexible selection of FB/I2C voltage regulation mode
  - Support I2C programming to control Output current limit
  - Automatic PFM/PWM mode
- **12bit High Precision ADC**
- **Port Connect Detection**
  - 1 adapter inserting detection point
  - 2 load inserting detection points
- **Low Quiescent Input Current**
  - Shutdown current down to 40uA
- **Path MOS Driver**
  - 3 NMOS drivers integrated
- **NTC Detection**
  - Support battery high and low temperature protection
  - Support IEC 62368 standard
- **Protection**
  - Input Over Voltage Protection
  - Output Over Voltage Protection
  - Output Over Current Protection
  - Output Short Protection
  - Thermal shutdown protection
- **I2C Interface**
- **QFN-32(4x4mm) Package**

4. Device Comparison Table

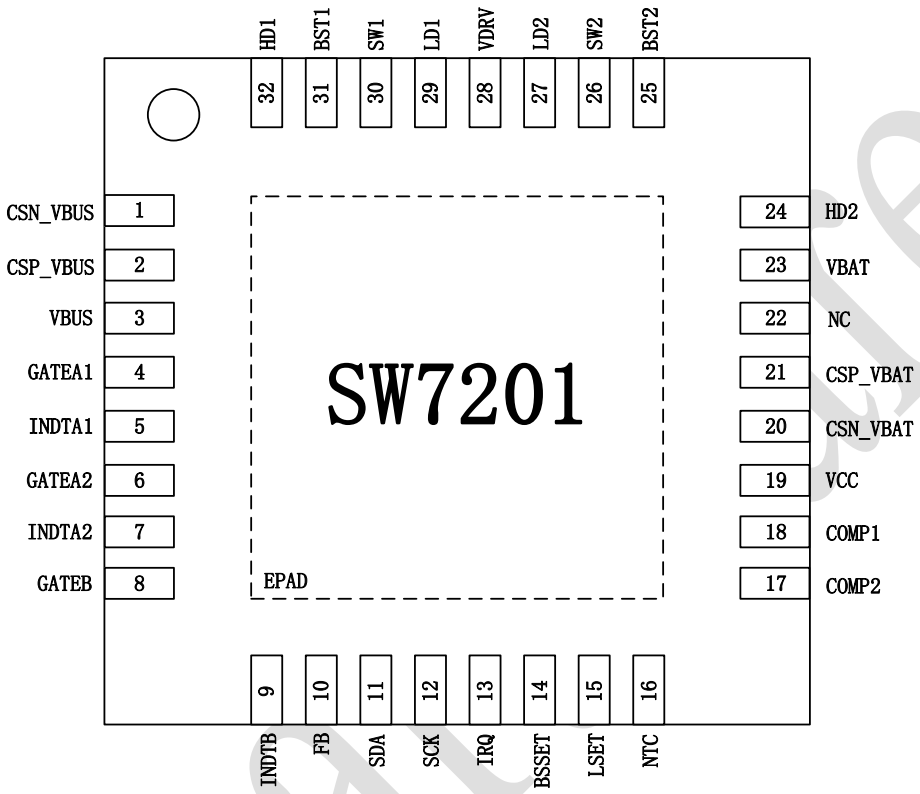
	SW7201	SW7203
Interface	I2C	I2C
Device Address	0x3C/0x38/0x1C/0x18	0x3C/0x38/0x1C/0x18
DCDC Topology	Buck-Boost	Buck-Boost
BATFET Power Path	No	Yes
Switching Frequency (Hz)	200K/300K/400K/800K	200K/300K/400K/800K
Cell Count	1s-4s	1s-4s
Charging Target Voltage Range	3V-19.2V	3V-19.2V
Input Voltage Range	4V-24V	4V-24V
Discharge Voltage Range	3V-22V	3V-22V

5. Functional Block Diagram



6. Pin Configuration and Functions

6.1. Pin Configuration



6.2. Pin Functions

Pin	Name	Function Description
1	CSN_VBUS	The current sensing negative pole on the VBUS side. In order to avoid the influence of high-frequency noise on the current sensing signal and to stabilize the current sensing, a 100nF capacitor needs to be added in parallel with the VBUS current sensing resistor, and a low-pass filter needs to be added between the current sensing resistor and CSN_VBUS. For the design of the low-pass filter, please refer to "11.2.4 VBUS current sensing low-pass filter parameter selection".
2	CSP_VBUS	The current sensing positive pole on the VBUS side. In order to avoid the influence of high-frequency noise on the current sensing signal and to stabilize the current sensing, a 100nF capacitor needs to be added in parallel with the VBUS current sensing resistor, and a low-pass filter needs to be added between the current sensing resistor and CSP_VBUS. For the

		design of the low-pass filter, please refer to "11.2.4 VBUS current sensing low-pass filter parameter selection".
3	VBUS	Chip power supply and VBUS voltage sensing.
4	GATEA1	NMOS power path transistor driver 1. This driver is enabled by a charge pump, which is weak in driving capability. When the path transistor drive is used, it is recommended to use an NMOS with gate source leakage current no greater than 100nA. The GATEA1 can remain floating without using the power path transistor drive.
5	INDTA1	Load inserting detection 1. When this function is used to detect load inserting, a ground capacitor of no less than 4.7uF must be set on INDTA1, and the recommended value of this capacitor is 10uF.
6	GATEA2	NMOS power path transistor driver 2. This driver is enabled by a charge pump, which is weak in driving capability. When the path transistor driver is used, an NMOS with gate source leakage current no greater than 100nA is recommended. The GATEA2 can remain floating without using the pass transistor drive.
7	INDTA2	Load inserting detection 2. When this function is used to detect load inserting, a grounded capacitor of no less than 4.7uF must be set on INDTA2, and the recommended value of this capacitor is 10uF.
8	GATEB	NMOS power path transistor driver 3. This driver is enabled by a charge pump, which is weak in driving capability. When the power path transistor driver is used, an NMOS with gate source leakage current no greater than 100nA is recommended. The GATEB can remain floating without using the power path transistor drive.
9	INDTB	Adapter inserting detection. When the external power supply and the VBUS are isolated by the power path transistor, the INDTB needs to be connected to the external power input port; when the external power supply and the VBUS are not isolated by the power path transistor, the INDTB needs to be shorted to the VBUS.
10	FB	External feedback of VBUS output voltage. The voltage of the FB is fixed at 0.5V. When the output voltage is not set with external feedback, the FB is floating.
11	SDA	I2C Data. Please connect SDA to the host controller or smart battery. 10KΩ pull-up resistors are recommended for SDA lines.

12	SCK	I2C Clock. Please connect SCL to the host controller or smart battery. 10KΩ pull-up resistors are recommended for SCL lines.
13	IRQ	I2C Interrupt. IRQ is for open-drain output. 10KΩ resistors are recommended. When the event interrupt is triggered, the IRQ output goes low until the event interrupt flag bit is cleared.
14	BSSET	Number of battery cells: 1-4 cells can be set: 1 cell for 10KΩ, 2 cells for 20KΩ, 3 cells for 30KΩ, and 4 cells for 43KΩ.
15	LSET	Inductance value setting: 4 different inductance values can be set: 1uH for 10KΩ, 2.2uH for 20KΩ, 3.3uH for 30KΩ, and 4.7uH for 43KΩ. This setting must be consistent with the external inductance value; otherwise the buck-boost cannot work normally.
16	NTC	Battery temperature sensing. The NTC thermistor must be a 103 resistor with a B value of 3435. For the specific protection threshold, please refer to " 10.5.2 Battery over-temperature protection". If the NTC over-temperature protection function is not needed, the NTC resistor can be replaced with a fixed 10KΩ resistor or the NTC protection can be turned off through a register.
17	COMP2	CC loop compensation. For the specific RC compensation network of COMP2, please refer to "11.2.3 COMP RC parameter selection".
18	COMP1	CV loop compensation. For the specific RC compensation network of COMP1, please refer to "11.2.3 COMP RC parameter selection"
19	VCC	5V linear regulator output provided by VBUS or VBAT. The 5V linear regulator is activated when the buck-boost is operating. VCC needs a 10uF ground capacitor near the VCC pin of the chip.
20	CSN_VBAT	The current sensing negative pole on the VBAT side; VBAT voltage sensing. In order to ensure the stability of current sensing, a 100nF capacitor needs to be added in parallel with the VBAT current sensing resistor.
21	CSP_VBAT	The current sensing positive pole on the VBAT side. In order to ensure the stability of current sensing, a 100nF capacitor needs to be added in parallel with the VBAT current sensing resistor.
22	NC	Floating.
23	VBAT	Chip power supply; VBAT voltage sensing.

24	HD2	VBAT side upper transistor gate drive. It needs to be connected to the gate of the high-side NMOS (Q4) of the half-bridge on the VBAT side.
25	BST2	VBAT side upper transistor bootstrap. A 100nF capacitor needs to be connected between SW2 and BST2. The bootstrap diodes of VDRV and BST2 are integrated inside the chip.
26	SW2	VBAT side switching point. SW2 needs to be connected to the source of the high-side NMOS (Q4) of the half-bridge on the VBAT side.
27	LD2	VBAT side lower transistor gate drive. It needs to be connected to the gate of the low-side NMOS (Q3) of the half-bridge on the VBAT side.
28	VDRV	5.5V linear regulator output provided by VBUS or VBAT. The 5.5V linear regulator is activated in standby mode and buck-boost operating mode. VDRV needs a 10uF ground capacitor near the VDRV pin of the chip.
29	LD1	VBUS side lower transistor gate drive. It needs to be connected to the gate of the low-side NMOS (Q2) of the half-bridge on the VBUS side
30	SW1	VBUS side switching point. SW1 needs to be connected to the source of the high-side NMOS (Q1) of the half-bridge on the VBUS side.
31	BST1	VBUS side upper transistor bootstrap. A 100nF capacitor needs to be connected between SW1 and BST1. The bootstrap diodes of VDRV and BST1 are integrated inside the chip.
32	HD1	VBUS side upper transistor gate. It needs to be connected to the gate of the high-side NMOS (Q1) of the half-bridge on the VBUS side.
/	EPAD	The grounded pad of the chip needs to be connected to the power ground plane to maintain proper connection between the EPAD and the PCB, thus ensuring its working performance and good heat dissipation.

7. Absolute Maximum Ratings

Parameters	Symbol	MIN	MAX	UNIT
VBUS Port Voltage	VBUS/FB/CSN_VBUS/ CSP_VBUS	-0.3	35	V
VBAT Port Voltage	CSN_VBAT/CSP_VBAT/ VBAT	-0.3	35	V
Switch Driver Voltage	HD1/HD2/BST1/BST2	-0.3	40	V
Switch Port Voltage	SW1/SW2	-0.3	35	V
Port Voltage	INDTB/INDTA1/INDTA2	-0.3	35	V
Path Control Voltage	GATEB/GATEA1/GATEA2	-0.3	40	V
Another pin voltages		-0.3	7	V
Junction temperature		-40	+150	°C
Storage temperature		-60	+150	°C
ESD（HBM）		-4	+4	KV

【Notice】Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maxi mum rated conditions for extended periods my affect device reliability.

8. Recommended Operating Conditions

Parameters	Symbol	MIN	Typical	MAX	UNIT
Input Voltage Range	VBUS	4		24	V
Battery Voltage Range	CSN_VBAT	3		19.2	V
Output Voltage Range	VBUS	3		22	V

9. Electrical Characteristics

（VBUS = 12V, VBAT = 10V, T_A = 25°C, unless otherwise specified.）

Parameters	Symbol	Test Conditions	MIN	TYP	MAX	UNIT
Power Supply						
VBUS input voltage	V_{INDTB}		4.4		24	V
VBUS input undervoltage threshold	V_{INDTB_UVLO}	INDTB voltage falling		4		V
VBUS input undervoltage hysteresis	$V_{INDTB\_UVLO\_HYS}$	INDTB voltage rising		400		mV
VDRV output voltage	V_{DRV}	Buck-Boost operating、Standby	5.3	5.5	5.7	V

		Shutdown		0		V
VDRV current limit	I_{VDRV}	Buck-Boost operating、Standby	35	50		mA
		Shutdown		0		mA
VCC output voltage	V_{CC}	Buck-Boost operating	4.8	5	5.2	V
		Standby、Shutdown		3.9		V
VCC current limit	I_{VCC}	Buck-Boost operating	90	120		mA
		Standby、Shutdown		10		mA
Charge Mode						
Trickle charge voltage range	V_{TC}	VBAT rising trickle_vol=0x00~0x6b	2.5		13.2	V
Trickle charge voltage	V_{TC}	trickle_vol=0x04	2.7	2.9	3	V
		trickle_vol=0x21	5.6	5.8	5.9	V
		trickle_vol=0x3E	8.5	8.7	8.8	V
		trickle_vol=0x5B	11.35	11.6	11.75	V
Trickle charge voltage hysteresis	V_{TC_HYS}	trickle_vol_hys=0x0		100		mV
		trickle_vol_hys=0x1		200		mV
		trickle_vol_hys=0x2		300		mV
		trickle_vol_hys=0x3		400		mV
Trickle charge current	I_{TC}	trickle_cur=0x0	50	100	250	mA
		trickle_cur=0x1	100	200	350	mA
		trickle_cur=0x2	200	300	450	mA
		trickle_cur=0x3	300	400	550	mA
VBUS constant charge current range	$I_{CC\_CHG\_VBUS}$	chg_ibus_limit=0x00~0x7f	0.5		6.85	A
VBUS constant charge current	$I_{CC\_CHG\_VBUS}$	chg_ibus_limit=0x00	0.35	0.5	0.75	A
		chg_ibus_limit=0x0A	0.9	1	1.3	A
		chg_ibus_limit=0x32	2.8	3	3.4	A
		chg_ibus_limit=0x5A	4.8	5	5.5	A
		chg_ibus_limit=0x78	6.3	6.5	7.1	A
VBAT constant charge current range	$I_{CC\_CHG\_VBAT}$	chg_ibat_limit=0x00~0x77	0.1		12	A
	$I_{CC\_CHG\_VBAT}$	chg_ibat_limit=0x04	0.45	0.5	0.65	A

VBAT constant charge current		chg_ibat_limit=0x13	1.9	2	2.2	A
		chg_ibat_limit=0x31	4.8	5	5.3	A
		chg_ibat_limit=0x4A	7.3	7.5	7.8	A
		chg_ibat_limit=0x63	9.7	10	10.4	A
Termination charge current	Iend	chg_end_cur=0x0	50	100	200	mA
		chg_end_cur=0x1	100	200	300	mA
		chg_end_cur=0x2	200	300	400	mA
		chg_end_cur=0x3	300	400	500	mA
Target charge voltage range	V_{CHG_VOL}	chg_vol=0x000~0x7ff	3		19.2	V
Target charge voltage	V_{CHG_VOL}	chg_vol=0x078	-1.2%	4.2	+1.2%	V
		chg_vol=0x21C	-1%	8.4	+1%	V
		chg_vol=0x3C0	-0.8%	12.6	+0.8%	V
		chg_vol=0x564	-0.8%	16.8	+0.8%	V
Recharge threshold	V_{RCHG}			V_{CHG_VOL}*97.3%		V
Trickle charge over time	T_{TC_OT}	chg_trk_overtime_set=0x0		0.5		H
		chg_trk_overtime_set=0x1		1		H
		chg_trk_overtime_set=0x2		2		H
		chg_trk_overtime_set=0x3		4		H
Constant charge over time	T_{CC_OT}	chg_cc_overtime_set=0x0		12		H
		chg_cc_overtime_set=0x1		24		H
		chg_cc_overtime_set=0x2		48		H
		chg_cc_overtime_set=0x3		72		H
Charging VBUS voltage limit protection threshold range	V_{HOLD}	chg_hold=0x00~0xff	4		20	V
Charging VBUS voltage limit protection threshold	V_{HOLD}	chg_hold=0x06	-2%	4.6	+2%	V
		chg_hold=0x2A	-2%	8.1	+2%	V
		chg_hold=0x46	-2%	11	+2%	V
		chg_hold=0x90	-2%	18.4	+2%	V
Discharge Mode						
VBUS output voltage range	V_{DISCHG_VOL}	I2C voltage regulation mode dischg_vbus=0x000~0x7ff	3		22	V

VBUS output voltage	V_{DISCHG_VOL}	I2C voltage regulation mode dischg_vbus=0x0C8	-3%	5	+3%	V
		I2C voltage regulation mode dischg_vbus=0x2BC	-2%	10	+2%	V
		I2C voltage regulation mode dischg_vbus=0x6A4	-2%	20	+2%	V
FB voltage	V_{FB}	FB voltage regulation mode	-2%	0.5	+2%	V
VBUS discharge current limit range	$I_{CC\_DISCHG\_VBUS}$	dischg_ibus_limit=0x00~0xff	0.5		6.85	A
VBUS discharge current limit	$I_{CC\_DISCHG\_VBUS}$	dischg_ibus_limit=0x00	0.4	0.5	0.7	A
		dischg_ibus_limit=0x0A	0.9	1	1.25	A
		dischg_ibus_limit=0x32	2.85	3	3.35	A
		dischg_ibus_limit=0x5A	4.8	5	5.4	A
		dischg_ibus_limit=0x78	6.3	6.5	7	A
VBAT discharge current limit range	$I_{CC\_DISCHG\_VBAT}$	dischg_ibat_limit=0x00~0x77	0.1		12	A
VBAT discharge current limit	$I_{CC\_DISCHG\_VBAT}$	dischg_ibat_limit=0x04	0.3	0.5	0.7	A
		dischg_ibat_limit=0x13	1.8	2	2.2	A
		dischg_ibat_limit=0x31	4.7	5	5.3	A
		dischg_ibat_limit=0x4A	7.1	7.5	7.9	A
		dischg_ibat_limit=0x63	9.5	10	10.5	A
VBAT input undervoltage threshold range	V_{BAT_UVLO}	bat_uvlo=0x00~0x77	2.7		13.2	V
VBAT input undervoltage threshold	V_{BAT_UVLO}	bat_uvlo=0x02	2.7	2.9	3.1	V
		bat_uvlo=0x1F	5.6	5.8	6	V
		bat_uvlo=0x3C	8.5	8.7	8.9	V
		bat_uvlo=0x59	11.4	11.6	11.8	V
VBAT input undervoltage hysteresis range	$V_{BAT\_UVLO\_HYS}$	bat_uvlo_hys=0x00~0x10	0.4		2	V
VBAT input undervoltage hysteresis	$V_{BAT\_UVLO\_HYS}$	bat_uvlo_hys=0x00		0.4		V
		bat_uvlo_hys=0x04		0.8		V
		bat_uvlo_hys=0x08		1.2		V
		bat_uvlo_hys=0x0C		1.6		V
Power On Reset						

VBUS power-up threshold	V_{VBUS_INIT}	INDTB short to VBUS		2.7		V
VBAT power-up threshold	V_{VBAT_INIT}			2.7		V
Quiescent Current						
Shutdown current	$I_{Q\_SHUTDOWN}$	Disable Load Inserting detection、Disable standby mode		40	80	uA
		Enable Load Inserting detection、Disable standby mode		50	100	uA
Standby current	$I_{Q\_STANDBY}$	Disable Load Inserting detection、Eaable standby mode		520	900	uA
		Enable Load Inserting detection、Eaable standby mode		530	920	uA
Quiescent current without load in discharge mode	I_{DISCHG_NOLOAD}	VBAT=12V、VBUS=5V、800KHz、Qg=5.5nC		1.9		mA
		VBAT=12V、VBUS=12V、800KHz、Qg=5.5nC		2.3		mA
		VBAT=12V、VBUS=20V、800KHz、Qg=5.5nC		3.4		mA
Switching						
Switching frequency	F_{SW}	Buck-Boost operating、freq=0x1	150	200	250	kHz
		Buck-Boost operating、freq=0x0	230	300	370	kHz
		Buck-Boost operating、freq=0x2	300	400	500	kHz
		Buck-Boost operating、freq=0x3	650	800	900	kHz
Abnormality protection						
Discharging VBUS overvoltage protection	$V_{VBUS\_DISCHG\_OVP}$	VBUS rising、I2C voltage regulation mode	V_{DISCHG_VOL}*109.5%	V_{DISCHG_VOL}*112.5%	V_{DISCHG_VOL}*115.5%	V
		VBUS falling、I2C voltage regulation mode		V_{DISCHG_VOL}*106%		V
		VBUS rising、FB voltage regulation mode	23.2	24	24.8	V
		VBUS falling、FB voltage regulation mode		22.7		V
Discharging VBUS overload protection	$V_{VBUS\_DISCHG\_OLP}$	VBUS falling、I2C voltage regulation mode		V_{DISCHG_VOL}*80%		V

		VBUS falling、FB voltage regulation mode		1.76		V
Discharging VBUS short-circuit protection	$V_{VBUS\_DISCHG\_SCP}$	VBUS falling		1.76		V
Discharging VBAT overvoltage protection	$V_{VBAT\_DISCHG\_OVP}$	VBAT rising	25.2	26	26.8	V
		VBAT falling		24.6		V
Charging VBUS overvoltage protection	$V_{VBUS\_CHG\_OVP}$	VBUS rising	25.2	26	26.8	V
		VBUS falling		24.6		V
Charging VBAT overvoltage protection	$V_{BAT\_CHG\_OVP}$	VBAT rising	V_{CHG_VOL}*102 %	V_{CHG_VOL}*104%	V_{CHG_VOL}*106%	V
		VBAT falling		V_{CHG_VOL}*102%		V
Battery high temperature protection in discharge mode	$T_{NTC\_DISCHG\_H}$	Discharge mode、Battery temperature rising、dischg_ntc_h=0		50		℃
		Discharge mode、Battery temperature rising、dischg_ntc_h=1		55		℃
		Discharge mode、Battery temperature rising、dischg_ntc_h=2		60		℃
		Discharge mode、Battery temperature rising、dischg_ntc_h=3		65		℃
Battery low temperature protection in discharge mode	$T_{NTC\_DISCHG\_L}$	Discharge mode、Battery temperature falling、dischg_ntc_l=0		-10		℃
		Discharge mode、Battery temperature falling、dischg_ntc_l=1		-5		℃
		Discharge mode、Battery temperature falling、dischg_ntc_l=2		0		℃
		Discharge mode、Battery temperature falling、dischg_ntc_l=3		-20		℃
Battery high temperature	$T_{NTC\_CHG\_H}$	Charge mode、		45		℃

protection in charge mode		Battery temperature rising、chg_ntc_h=0				
		Charge mode、Battery temperature rising、chg_ntc_h=1		40		℃
		Charge mode、Battery temperature rising、chg_ntc_h=2		50		℃
		Charge mode、Battery temperature rising、chg_ntc_h=3		55		℃
Battery low temperature protection in charge mode	$T_{NTC\_CHG\_L}$	Charge mode、Battery temperature falling、chg_ntc_l=0		0		℃
		Charge mode、Battery temperature falling、chg_ntc_l=1		10		℃
		Charge mode、Battery temperature falling、chg_ntc_l=2		5		℃
		Charge mode、Battery temperature falling、chg_ntc_l=3		-5		℃
NTC voltage detection accuracy	V_{NTC}	V_{NTC} >0.5V	-4%		+4%	V
		V_{NTC}≤0.5V	20		20	mV
Thermal shutdown threshold	T_{DIE_OTP}	Chip temperature rising		150		℃
Thermal shutdown hysteresis	$T_{DIE\_OTP\_HYS}$	Chip temperature falling		20		℃
Automatic Detection（BSSET&LSET）						
Detection threshold of 4 batteries	V_{BSSET_4S}		1.75		2.5	V
Detection threshold of 3 batteries	V_{BSSET_3S}		1.25		1.75	V
Detection threshold of 2 batteries	V_{BSSET_2S}		0.75		1.25	V
Detection threshold of 1 batteries	V_{BSSET_1S}		0.25		0.75	V

Detection threshold of 4.7UH inductance	$V_{LSET\_4.7UH}$		1.75		2.5	V
Detection threshold of 3.3UH inductance	$V_{LSET\_3.3UH}$		1.25		1.75	V
Detection threshold of 2.2UH inductance	$V_{LSET\_2.2UH}$		0.75		1.25	V
Detection threshold of 1UH inductance	V_{LSET_1UH}		0.25		0.75	V
I2C						
I2C Clock frequency	F_{I2C_CLK}			100	400	kHz
I2C pulse width low	V_{IL}				0.75	V
I2C pulse width high	V_{IH}		1.2			V

10. Function Description

SW7201 is a high-efficiency synchronous 4-transistor bidirectional buck-boost charge-discharge controller that supports the charge-discharge management of 1-4 cells. It can provide up to 100W output power.

10.1. Power-Up Sequence

10.1.1. Power up sequence from VBAT

In the case that the battery is connected without external power supply, the SW7201 draws power from VBAT, and starts power-on initialization. After the power-on initialization is completed, the SW7201 works in a low-power mode by default, and enters the shutdown state soon after. Low power mode can be turned off through registers.

10.1.2. Power up sequence from VBUS

When the battery is in dead battery state and INDTB and VBUS are shorted, the external power is supplied to VBUS. The SW7201 draws power from VBUS and starts power-on initialization. When there is external power supplied to VBUS, the SW7201 will not enter the shutdown state even if it is in the low-power mode.

If INDTB is not shorted with VBUS, the INDTB and VBUS shall be greater than V_{INIT_VBUS} at the same time for the SW7201 to be powered on and started.

10.2. Buck-Boost

Under different VBUS and VBAT voltages, the SW7201 will automatically work in three modes: buck, buck-boost, and boost. The three modes can be switched seamlessly, and there will be no sudden change in VBUS or VBAT voltage in the switching process. In addition, the SW7201 supports PFM/PWM. Under light load, it works in the PFM mode; under heavy load, it works in the PWM mode. At the same time, SW7201 supports 4 inductance values (1uH, 2.2uH, 3.3uH and 4.7uH) and 4 switching frequencies (200K, 300K, 400K and 800K), which can be flexibly adjusted according to the performance needs in actual applications.

10.2.1. Pulse frequency modulation (PFM)

In order to improve the efficiency at light load, the SW7201 will work in the PFM mode. The actual switching frequency will decrease when the charging power and discharging power decrease. When the average inductor current reaches the PWM mode set value, the SW7201 will switch from PFM to PWM.

In addition, although working in the PFM mode improves the light-load efficiency, the output ripple will increase accordingly. For applications that are sensitive to output ripple, the forced PWM mode can be set through the register. In the forced PWM mode, the SW7201 will not enter PFM even when operating at light load.

10.2.2. Pulse width modulation (PWM)

When operating in the PWM mode, at the beginning of a cycle, when the output of the error

amplifier is higher than the ramp voltage, the high-side NMOS of the half-bridge will be turned on; and when the output of the error amplifier falls below the ramp voltage, the low-side NMOS of the half-bridge will be turned on. At the end of the cycle, the ramp voltage is reset and ready to start the next cycle. In the process of switching on the MOS, the principle of "turning off before turning on" must be always followed to avoid the dangerous situation that high-side and low-side NMOS transistors are both on. With both the high-side and low-side NMOS transistors off, the inductor current is maintained by the body diodes of the high-side or low-side NMOS transistors.

The following table shows the operating states of the four power MOS transistors Q1-Q4 in the PWM mode.

Charge Mode			
Mode	Buck	Buck-Boost	Boost
Q1	Switching	Switching	On
Q2	Switching	Switching	Off
Q3	Off	Switching	Switching
Q4	On	Switching	Switching

Discharge Mode			
Mode	Buck	Buck-Boost	Boost
Q1	On	Switching	Switching
Q2	Off	Switching	Switching
Q3	Switching	Switching	Off
Q4	Switching	Switching	On

10.3. Charge settings

The SW7201 supports charging target voltage setting in the range of 3V-19.2V, and trickle charging setting in the range of 2.5V-13.2V. Therefore, it can support many different types of batteries.

Meanwhile, the SW7201 can be set to two modes (auto stop charging and continuous charging), to be compatible with the needs of more applications. It supports both dead battery start and no-battery working modes.

10.3.1. Start charging

When external power is connected, you can set and enter the charging state by the following sequence:

(1) Set the charging target voltage and the constant current charging current on the VBUS/VBAT side.

(2) Set the trickle charging threshold and trickle charging current.

(3) Set the input voltage limiting threshold.

(4) Make sure INDTB and VBUS are shorted.

(5) Enable the charging.

10.3.2. Trickle charging

When the battery voltage is lower than the trickle charging voltage threshold, it enters the trickle charging state. The charging current is controlled by the trickle charging current threshold.

The trickle charging threshold can be set through the register trickle_vol[6:0] in the range of 2.5V-13.2V (0.1V/step). When trickle_vol[6:0]=0x00, the trickle charging threshold is 2.5V. When the set value is greater than 13.2V, the trickle charging threshold remains unchanged at 13.2V. When the chip is powered on, it will automatically set the trickle charging threshold to the number of battery cells * 2.9V by detecting the setting result of the BSSET pin.

The trickle charging hysteresis can be set through the register trickle_vol_hys[1:0], and the value can be set to 0.1V/0.2V/0.3V/0.4V. When the chip is powered on, it will automatically set the trickle charging hysteresis to the number of battery cells * 0.1V by detecting the setting result of the BSSET pin.

The trickle charging current can be set through the register trickle_cur[1:0], and the value can be set to 100mA/200mA/300mA/400mA.

10.3.3. Constant current charging mode

When the battery voltage is higher than the trickle charging threshold at the same time, it enters the constant current charging mode. At this time, the charging current is limited by the VBUS/VBAT constant current charging current.

In the constant current charging mode, the charging current limit on the VBUS side and that on the VBAT side take effect at the same time. After the charging parameters are set and the charging enable bit is turned on, the soft-start of the charging current begins. After the charging current increases to the charging current threshold on the VBUS side or that on the VBAT side, the charging currents will no longer increase. The trickle charging current limit only limit the VBAT charging current, while the VBUS current is not limited at this time.

The VBUS constant current charging current can be set through the register chg_ibus_limit[6:0] in the range of 0.5A-6.85A (50mA/step). When chg_ibus_limit[6:0]=0x00, the VBUS constant current charging current is set to 0.5A.

The VBAT constant current charging current can be set through the register chg_ibat_limit[6:0] in the range of 0.1A-12A (100mA/step). When chg_ibat_limit[6:0]=0x00, the VBAT constant current charging current is set to 0.1A. When the set value of the register is greater than 12A, the VBAT constant current charging current remains unchanged at 12A.

10.3.4. Constant voltage charging mode

During the constant current charging process, the VBAT voltage continues to rise, and when the VBAT voltage rises to the charging target voltage, it enters the constant voltage charging mode. At this time, the VBAT voltage remains constant, and as the battery voltage continues to rise, the charging current will gradually decrease.

If the charger done function is enabled, when the VBAT charging current is lower than the charging terminate current threshold, the charger done will be triggered and the charging will be turned off. As the external power supply stays on, if the battery voltage gradually falls back below the recharge threshold, it will be turned back on for charging.

If the charger done function is disabled, then the charging loop will control the VBAT voltage to stay at the charging target voltage and keep charging, and will no longer judge whether the VBAT

charging current is lower than the charging terminate current threshold.

The charging target voltage can be set through the register chg_vol[10:0] in the range of 3V-19.2V (10mV/step). When chg_vol[10:0]=0x000, the charging target voltage is set to 3V. When the set value is greater than 19.2V, the charging target voltage remains unchanged at 19.2V. When the chip is powered on, it will automatically set the charging target voltage to the number of battery cells * 4.2V by detecting the setting result of the BSSET pin.

The charge terminate current can be set through the register chg_end_cur[1:0], and the value can be set to 100mA/200mA/300mA/400mA.

The recharge threshold is fixed at 97% of the charge target voltage.。

10.4. Discharge settings

The SW7201 supports the external FB voltage regulation and internal I2C voltage regulation, and it is compatible with different protocol chips.

10.4.1. Start discharging

You can start discharging by following the steps below:

(1) Set the output voltage. (This step can be ignored in the case of external FB voltage regulation)

(2) Set the VBUS/VBAT output current limit value.

(3) Set the battery undervoltage threshold and battery undervoltage hysteresis.

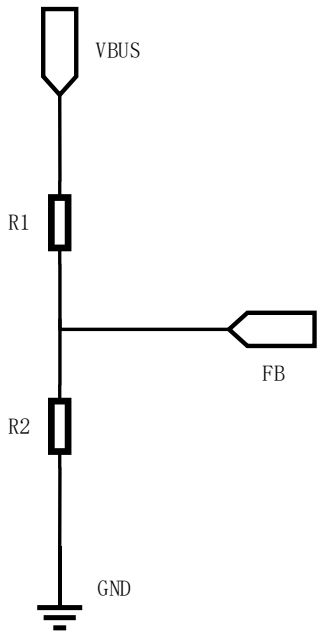
(4) Enable the discharge.

10.4.2. FB voltage regulation

In the external FB voltage regulation mode, the voltage of the FB pin is fixed at 0.5V, and an appropriate voltage divider can be selected according to the required output voltage. 100K is recommended for R1. After setting the output current limit and battery undervoltage threshold, the output can be turned on by enabling the discharge enable bit.

In the FB mode, the output voltage is calculated as follows：

$$\mathrm{VBUS} = 0.5 \times (1 + \frac{R1}{R2})$$



For the settings of output current limit and battery undervoltage threshold, please refer to "10.4.3

I2C voltage regulation" for details.

10.4.3. I2C voltage regulation

In the internal I2C voltage regulation mode, the FB pin is in the floating state, and there is no need to add an FB resistor. After setting the output voltage, output current limit and battery undervoltage threshold, the output can be turned on by enabling the discharge enable bit.

The VBUS output voltage can be set through the register discchg_vbus[10:0] in the range of 3V-22V (10mV/step). When discchg_vbus[10:0]=0x000, the VBUS output voltage is set to 3V. When the set value of the register is greater than 22V, the VBUS output voltage remains unchanged at 22V.

The VBUS current limit can be set through the register discchg_ibus_limit[6:0] in the range of 0.5A-6.85A (50mA/step). When dischg_ibus_limit[6:0]=0x00, the VBUS current limit is set to 0.5A.

The VBAT current limit can be set through the register discchg_ibat_limit[6:0] in the range of 0.1A-12A (100mA/step). When dischg_ibat_limit[6:0]=0x00, the VBAT current limit is set to 0.1A. When the set value of the register is greater than 12A, the VBAT current limit remains unchanged at 12A.

The battery undervoltage threshold can be set through the register bat_uvlo[6:0] in the range of 2.7V-13.2V, 0.1V/step. When bat_uvlo[6:0]=0x00, the battery undervoltage threshold is set to 2.5V. When the set value of the register is greater than 13.2V, the battery undervoltage threshold remains unchanged at 13.2V. When the chip is powered on, the battery undervoltage threshold is automatically set to 3.0V.

The battery undervoltage hysteresis can be set through the register bat_uvlo_hys[1:0], and the settable value is 0.4V-2V (0.1V/step) . When bat_uvlo_hys[1:0]=0x00, the battery undervoltage hysteresis is set to 0.4V.

10.5. Abnormality protection

The SW7201 is designed with effective protection measures, including thermal shutdown protection, Battery over-temperature protection, output/input VBUS overvoltage protection, VBAT overvoltage protection, cycle-by-cycle peak overcurrent protection, charging VBUS undervoltage protection, discharging VBAT undervoltage protection, discharging VBUS short-circuit protection, discharging overcurrent protection, trickle charging timeout protection and constant current charging timeout protection, etc., to ensure the safety of charging and discharging equipment to the greatest extent.

10.5.1. Thermal shutdown protection

The SW7201 supports thermal shutdown protection. When its temperature rises to the thermal shutdown protection threshold and lasts for more than 16ms, it is considered that the chip over-temperature abnormality is triggered and the buck-boost will be turned off. There are 4 levels of chip over-temperature temperature for selection: 120°C/130°C/140°C/150°C. After the chip over-temperature protection is triggered, as long as the chip temperature drops to the thermal shutdown threshold -20°C and lasts for more than 16mS, the chip will exit the thermal shutdown and the buck-boost will restart.

10.5.2. Battery over-temperature protection

The SW7201 supports battery over-temperature protection. It can monitor the battery temperature

in real time, and triggers protection when the temperature is abnormal. The NTC Pin calculates the current battery temperature by discharging a certain amount of current to the NTC resistor and then collecting the NTC voltage. The NTC function supports 103AT resistors. When the resistance value of NTC resistor is low, 80uA is discharged, when the resistance value of NTC resistor is medium, 40uA is discharged, and when the resistance value of NTC resistor is high, 20uA is discharged to ensure sufficient detection range and accuracy.

In the charging state, when he battery temperature is detected to be lower than the charging low-temperature protection threshold or higher than the charging high-temperature protection threshold and lasts for more than 16ms, it is considered that the charging NTC over-temperature abnormality is triggered and the charger will be turned off. After the NTC over-temperature abnormality occurs, if the battery temperature returns to the charging low-temperature protection threshold +5°C or the charging high-temperature protection threshold -5°C and lasts for more than 16ms, the Battery over-temperature protection will be exited and the charger will be resumed.

In the discharging state, when the battery temperature is detected to be lower than the discharging low-temperature protection threshold or higher than the discharging high-temperature protection threshold and lasts for more than 16ms, it is considered that the discharging NTC over-temperature abnormality is triggered, the discharging will be turned off. After the NTC over-temperature abnormality occurs, if the battery temperature returns to the discharging low-temperature protection threshold +5°C or the discharging high-temperature protection threshold -5°C and lasts for more than 16ms, the battery over-temperature protection will be exited and the discharging will resume operation.

The following protection thresholds are optional:

(1) Charging low temperature protection threshold: 10℃, 5℃, 0℃, -5℃.

(2) Charging high temperature protection threshold: 40℃, 45℃, 50℃, 55℃.

(3) Discharging low temperature protection threshold: -20℃, -10℃, -5℃, 0℃.

(4) Discharging high temperature protection threshold: 50℃, 55℃, 60℃, 65℃.

If the NTC protection is not needed, please replace the 103AT with a 10K resistor or turn off the NTC protection function through the register. When the NTC function is turned off through the register, the 62368 temperature protection needs to be turned off at the same time.

The NTC resistance value and NTC voltage corresponding to the specific temperature are as follows:

temperature /℃	NTC resistance /k	NTC voltage/V	NTC current/uA
-25	86.43	1.728	20
-20	67.77	1.355	20
-15	53.41	1.068	20
-10	42.47	1.698	40
-5	33.9	1.356	40
0	27.28	1.091	40
5	22.05	1.764	80
10	17.96	1.436	80
15	14.69	1.175	80
20	12.09	0.967	80
25	10.00	0.800	80
30	8.313	0.665	80
35	6.940	0.555	80

40	5.827	0.466	80
45	4.911	0.392	80
50	4.160	0.332	80
55	3.536	0.282	80
60	3.020	0.241	80
65	2.588	0.207	80

10.5.3. Discharging VBUS overvoltage protection

The SW7201 supports discharging VBUS overvoltage protection. When the output voltage exceeds the discharging VBUS overvoltage protection threshold and lasts for more than 16ms, it is considered that the discharging VBUS overvoltage abnormality is triggered, and the discharge will be turned off. After triggering the discharging VBUS overvoltage abnormality, when the output voltage is lower than the discharging VBUS overvoltage exit threshold for more than 16ms, the discharging VBUS overvoltage abnormality will be exited and the discharge will be resumed.

In the FB voltage regulation mode, the discharging VBUS overvoltage protection threshold is 24V, and the discharging VBUS overvoltage exit threshold is 22.74V.

In the I2C voltage regulation mode, the discharging VBUS overvoltage protection threshold is 112% of the set output voltage, and the discharging VBUS overvoltage exit threshold is 106% of the set output voltage.

10.5.4. Discharging VBUS overload protection

The SW7201 supports VBUS overload protection in discharge mode, which can turn off the output when the output is overloaded. When the VBUS discharging voltage is lower than the discharging VBUS overcurrent protection threshold and lasts for 32ms, it is considered that the discharging VBUS overcurrent abnormality is triggered and the discharge will be turned off.

In the FB voltage regulation mode, the discharging VBUS overcurrent protection threshold is consistent with the short-circuit protection threshold, i.e., 1.76V.

In the I2C voltage regulation mode, the discharging VBUS overcurrent protection threshold is 80% of the set output voltage.

10.5.5. Discharging VBUS short-circuit protection

The SW7201 supports discharging VBUS short-circuit protection, which can turn off the buck-boost output when a short circuit occurs at the output. When the VBUS output voltage is lower than the output VBUS short-circuit protection threshold and lasts for more than 4ms, it is considered that the discharging VBUS short-circuit abnormality is triggered, and the discharge will be turned off.

The output VBUS short-circuit protection threshold is 1.76V.

10.5.6. Discharging VBAT undervoltage protection

The SW7201 supports discharging VBAT undervoltage protection, which can turn off the buck-boost output and stop external discharge when the battery is low. When the battery voltage is lower than the VBAT undervoltage protection threshold and lasts for more than 32ms, it is considered that the discharging VBAT undervoltage abnormality is triggered and the discharge will be turned off. When the battery voltage is higher than the VBAT undervoltage protection threshold plus the VBAT undervoltage protection hysteresis and lasts for more than 64ms, the discharging VBAT undervoltage

abnormality will be terminated and the discharge will be resumed.

The VBAT undervoltage protection threshold can be set through the register in the range of 2.7V~13.2V (0.1V/step), and the default value is 3V. The VBAT undervoltage protection hysteresis can be set in the range of 0.4V~2V (0.1V/step), and the default value is 0.4V.

10.5.7. Discharging VBAT overvoltage protection

The SW7201 supports discharging VBAT overvoltage protection, which can prohibit the discharge in the case of overvoltage at the VBAT input. When the battery voltage is higher than the discharging VBAT overvoltage protection threshold and lasts for more than 100us, it is considered that the discharging VBAT overvoltage abnormality is triggered and the discharge will be turned off. After triggering the discharging VBAT overvoltage protection, when the battery voltage is lower than the discharging VBAT overvoltage recovery threshold and lasts for more than 36ms, it is considered that the discharging VBAT overvoltage abnormality is terminated.

The discharging VBAT overvoltage protection threshold is 26V, while the discharging VBAT overvoltage recovery threshold is 24.63V.

10.5.8. Cycle-by-cycle peak overcurrent protection

The SW7201 supports cycle-by-cycle peak overcurrent protection. During the operation of the buck-boost, if the peak inductor current exceeds 12A/14A/16A/18A, the active transistor in the current mode will be turned off in advance to limit the peak inductor current.

When working in the discharging boost mode, the SW7201 detects the peak current of the inductor with the Vds of Q2 and complete the cycle-by-cycle peak overcurrent protection. It is required to set the register of the on-resistance of Q2 according to the actual on-resistance of Q2 to ensure the actual detected peak current limit of the inductor to be closer to the inductor peak current value set by the register. The register of the on-resistance of Q2 can be set to 2.5mΩ/5mΩ/7.5mΩ/10mΩ. The actual peak current limit value in the discharging boost mode is as follows.

$$I_{OCP\_ACT} = \frac{R_{DSON\_Q2\_SET}}{R_{DSON\_Q2\_ACT}} \times I_{OCP\_SET}$$

wherein I_{OCP_ACT} is the actual peak current limit value, $R_{DSON\_Q2\_ACT}$ is the actual on-resistance of Q2, $R_{DSON\_Q2\_SET}$ is the on-resistance of Q2 set by the register, and I_{OCP_SET} is the peak current limit value set by the register.

The inductor peak current is set for both charging and discharging. If charging and discharging require different peak overcurrent protection thresholds, please set the corresponding value before enabling the discharge/charge mode.

10.5.9. Charging VBUS overvoltage protection

The SW7201 supports charging VBUS overvoltage protection, which can prohibit the charge in case of overvoltage at the VBUS input. When the VBUS voltage is higher than the charging VBUS overvoltage protection threshold for 100us, it is considered that the charging VBUS overvoltage abnormality is triggered. After triggering the charging VBUS overvoltage abnormality, when the VBUS voltage is lower than the charging VBUS overvoltage exit threshold for 4ms, it is considered that the charging VBUS overvoltage abnormality is exited.

The charging VBUS overvoltage protection threshold is 26V, while the charging VBUS overvoltage exit threshold is 24.63V.

10.5.10. Charging VBUS voltage limit protection

The SW7201 supports charging VBUS voltage limit protection. When the input voltage drops to the charging VBUS voltage limit protection threshold due to insufficient load capacity of the external power supply, the SW7201 will automatically decrease the charging current to ensure that the charge can continue.

The charging VBUS voltage limit protection threshold can be set through the register in the range of 4V-20V (0.1V/step).

10.5.11. Charging VBAT overvoltage protection

The SW7201 supports charging VBAT overvoltage protection, which can prohibit the charge when the battery voltage is too high. When the battery voltage exceeds 104% of the charging target voltage and lasts for more than 16ms, it is considered that the charging VBAT overvoltage abnormality is triggered, the buck-boost will be turned off, and the 20mA drain path from VBAT to GND will be opened for 16ms for every 64ms. After the charging VBAT overvoltage abnormality is triggered, when the battery voltage is lower than 102% of the charging target voltage and lasts for more than 16ms, it is considered that the charging VBAT overvoltage abnormality is exited.

For the setting of the charging target voltage, please refer to "10.3.4 Constant voltage charging mode".

10.5.12. Charge timeout protection

The SW7201 supports charge timeout protection, which can prohibit the charge in the case of charge timeout. The charge timeout is divided into trickle charging timeout and constant current charging timeout, and different thresholds can be set respectively:

(1) Trickle charging timeout threshold: 30min/1h/2h/4h.

(2) Constant current charge timeout threshold: 12h/24h/48h/72h.

The charge timeout protection function can be turned off through the register.

10.6. ADC

The SW7201 has a built-in 12bit ADC, which can collect data such as VBUS/VBAT/IBUS/IBAT. The specific calculation formula is as follows.

Channel	Description	Dynamic range	Calculation formula (N is the ADC output code value)
Vbat	VBAT voltage	0V-30.72V	Vbat=N*7.5mV
Vbus	VBUS voltage	0V-30.72V	Vout=N*7.5mV
Ibat_chg	VBAT charging current	0A-20.48A	Ibat_chg=N*5mA
Ibat_dischg	VBAT discharging current	0A-20.48A	Ibat_dischg=N*5mA
Ibus_chg	VBUS charging current	0A-20.48A	Iout_chg=N*5mA
Ibus_dischg	VBUS discharging current	0A-20.48A	Iout_dischg=N*5mA
Tdie	On-chip temperature	-100℃~200℃	Tdiet=(N-1839)/6.82℃
Vntc	NTC voltage	-25℃~65℃	Refer to "9.6.2 NTC over-temperature protection"

10.7. 62368 battery temperature protection

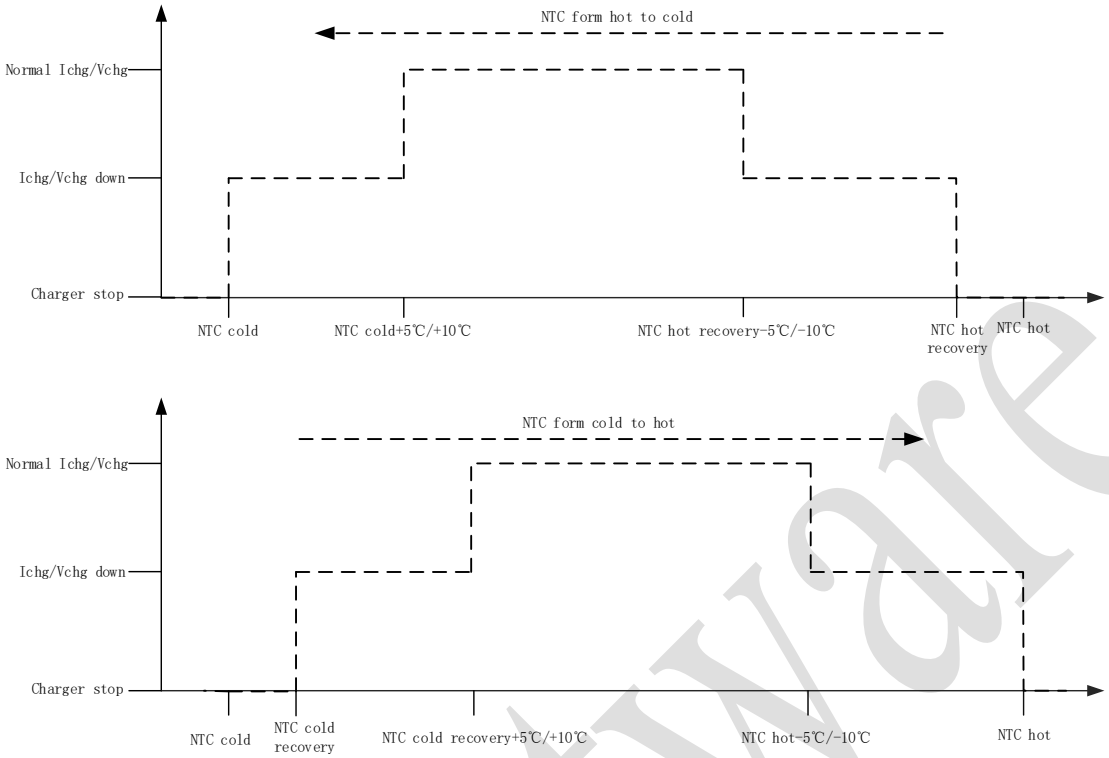
The SW7201 integrates the 62368 battery temperature protection function, which can be activated during charging. The specific methods are as follows:

(1) Room temperature -> Low temperature: When the battery temperature decreases to the charger's low temperature protection threshold +5°C/+10°C (can be set to 2 levels: +5°C/+10°C, through the register), the charging current is reduced to 50%/25% of the set current limit (can be set to 3 levels: 50 %/25%/no reduction, through the register). At the same time, the charging target voltage is reduced by 0.1V * the number of battery cells (can be set to 2 levels: 0.1V/no reduction); when the battery temperature decreases to the charger's low temperature protection threshold, the charger will be turned off.

(2) Low temperature -> Room temperature: After NTC turns off the charger due to low temperature, when the battery temperature rises to the charger's low temperature protection threshold +5°C, the charge will be resumed. However, the charging current is 50%/25% of the set current limit, and the charging target voltage is reduced by 0.1V; when the battery temperature rises to the charger's low temperature recovery threshold +5°C/+10°C, the charging current and charging target voltage will both recover to the set value.

(3) Room temperature -> High temperature: When the battery temperature rises to the charger's high temperature protection threshold -5°C/-10°C (can be set to 2 levels: -5°C/-10°C through the register), the charging target voltage will be reduced by 0.1V (can be set to 2 levels: 0.1V/no reduction); when the battery temperature rises to the charger's high temperature protection threshold, the charger will be turned off.

(4) High temperature -> Room temperature: After NTC turns off the charger due to high temperature, when the battery temperature drops to the charger's high temperature protection threshold -5°C, the charge will be resumed, and the charging target voltage will be reduced by 0.1V * the number of battery cells; when the battery temperature drops to the charger's high temperature recovery threshold -5°C/-10°C, the charging target voltage will recover to the set value.



10.8. IRQ

The SW7201 integrates the external interrupt pin IRQ in an open-drain structure. When it is used, a 10K resistor is recommended to pull up. When an event that needs to be monitored occurs, the IRQ will pull low and remain low until the flag bit of the corresponding event is cleared.

The events that can be monitored include adapter input pull-out, load detection trigger and operation abnormality. Each event can be individually set through registers.

10.9. Inserting detection

The SW7201 integrates two-channel load inserting detection, so that it can automatically identify external load inserting when it is turned on, which simplifies the solution design.

When inserting detection is turned on, the voltage on the corresponding port will be established above the detection threshold, and the load inserting will pull down this voltage to below the identification threshold, thereby identifying the device inserting.

After each inserting detection is triggered, if you want to continue to identify the external load inserting, you need to turn off the inserting detection and then turn it on again to take effect.

10.10. Power path transistor driver

The SW7201 integrates 3 NMOS power path transistor drivers, each of which can be turned on and off independently without adding any external circuit, which simplifies the design.

10.11. I2C

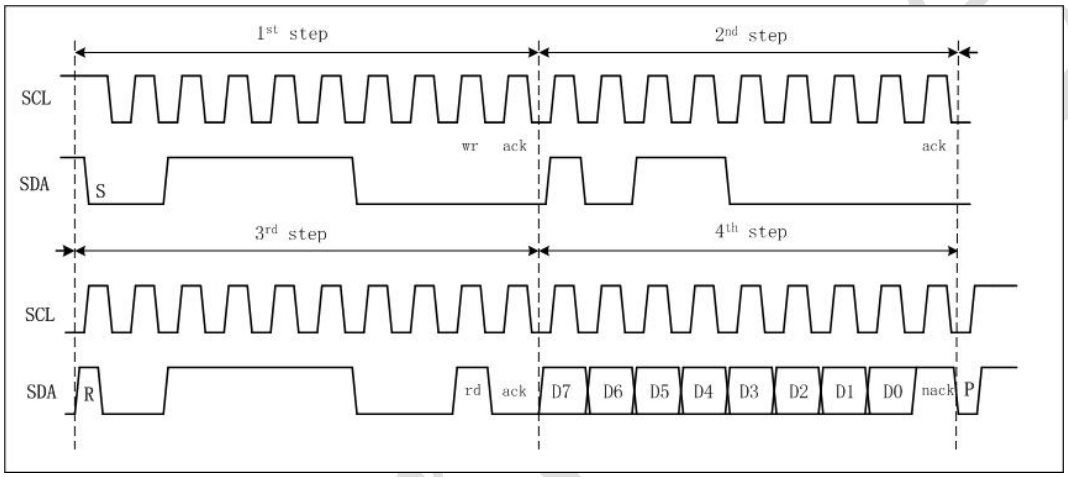
The SW7201 supports I2C interface and 100K-400K transmission rate. The master can read the status information of the chip through the I2C interface. And the SW7201 supports 4 different I2C addresses: 0x3C/0x38/0x1C/0x18.

I2C does not support continuous read/write.

Read:

Slave address: 0x3C (read 0x79, write 0x78)

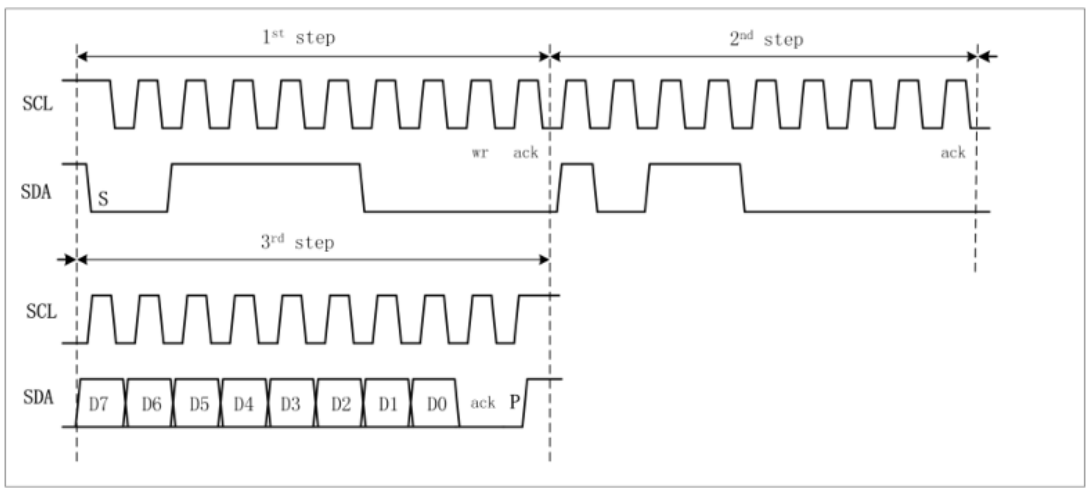
Register address: 0xB0



Write:

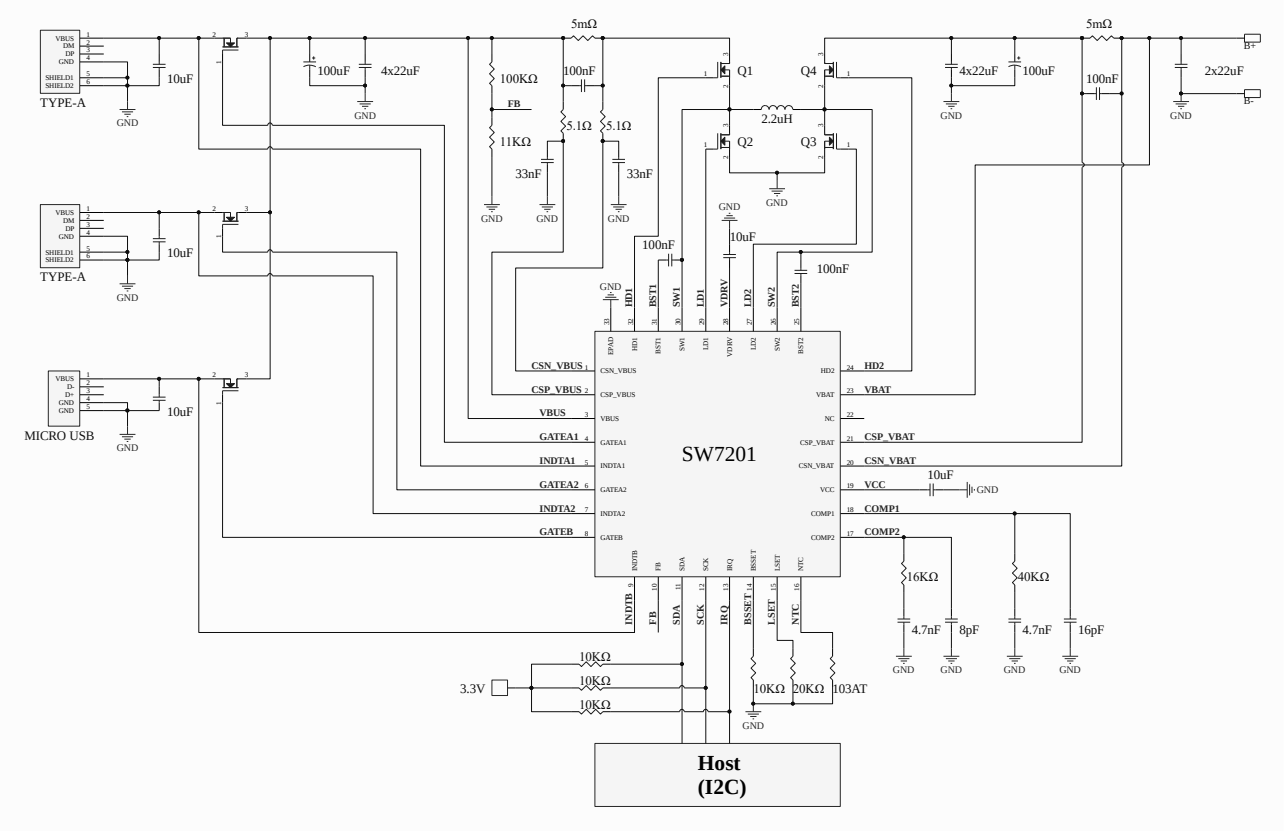
Slave address: 0x3C (read 0x79, write 0x78)

Register address: 0xB0



11. Application and Implementation

11.1. Typical Application



11.2. Parameter configuration

11.2.1. Battery cell configuration

The BSSET is connected to ground with different resistors for configuring the number of battery cells. Please refer to the table below for specific resistor settings.

BSSET resistor	Number of battery cells
10K	1
20K	2
30K	3
43K	4

11.2.2. Inductor value selection

LSET is connected to ground with different resistors for configuring the inductors. When the switching frequency is 800K, 1uH or 2.2uH inductors can be selected and 100uF solid state capacitors are recommended for CSP_VBAT and VBUS. When the switching frequency is 200K/300K/400K,

3.3uH or 4.7uH inductors are recommended and the solid state capacitors for CSP_VBAT and VBUS should be increased to 220uF.

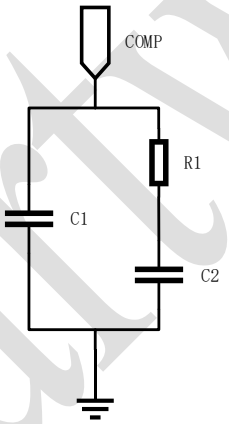
Please refer to the table below for specific resistor settings of the LSET.

LSET resistor	Inductor value
10K	1uH
20K	2.2 uH
30K	3.3 uH
43K	4.7 uH

11.2.3. COMP RC parameter selection

Different resistance and capacitance parameters should be selected for the COMP1 and COMP2 pins according to different inductances. COMP1 is the CV loop compensation pin, while COMP2 is the CC loop compensation pin.

COMP compensation circuit:



Specific settings of COMP1:

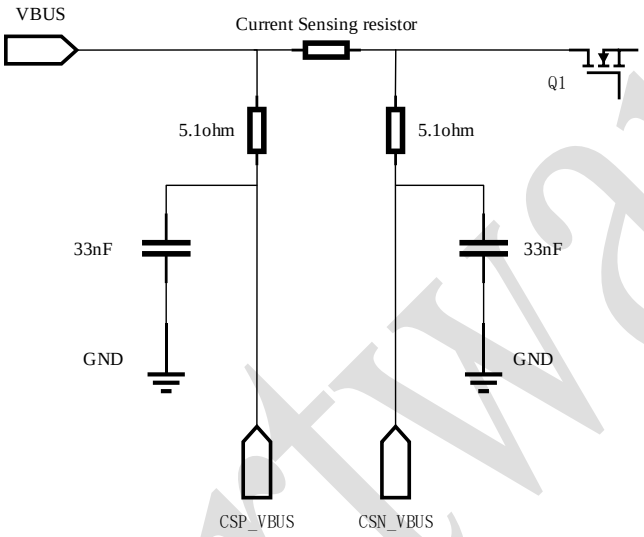
Inductor value	R1	C1	C2
1uH	60K	16pF	4.7nF
2.2 uH	40K	16pF	4.7nF
3.3 uH	30K	16pF	4.7nF
4.7 uH	20K	16pF	4.7nF

Specific settings of COMP2:

Inductor value	R1	C1	C2
1uH	8K	8pF	4.7nF
2.2 uH	16K	8pF	4.7nF
3.3 uH	24K	8pF	4.7nF
4.7 uH	32K	8pF	4.7nF

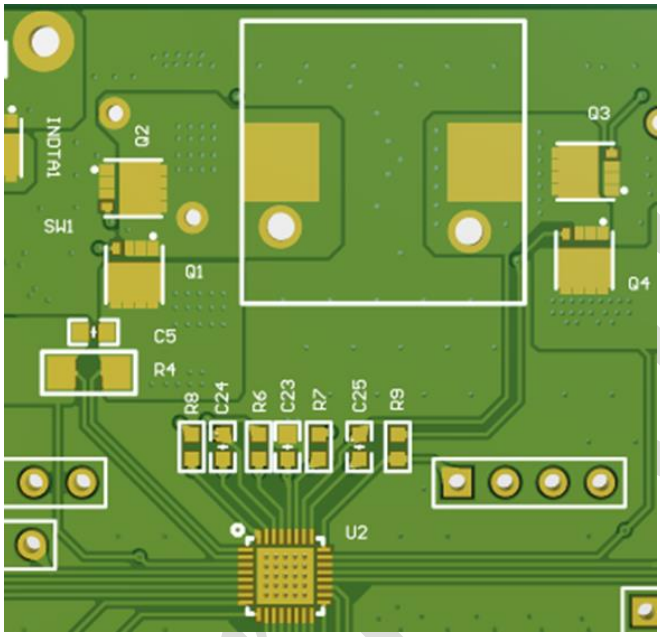
11.2.4. VBUS current sensing low-pass filter parameter selection

The SW7201 is designed based on the average current mode and it monitors the inductor current through the VBUS current sensing resistors. The parasitic inductance on the PCB leads to high-frequency noise on CSN_VBUS-CSP_VBUS, which affects the current sensing. When the time constant of the low-pass filter is between 47ns and 200ns, it can filter out high-frequency noise sufficiently, and will not cause too much delay to the current sensing signal, thus ensuring stable operation. The filter circuit shown in the figure below is recommended to be added on CSN_VBUS and CSP_VBUS.

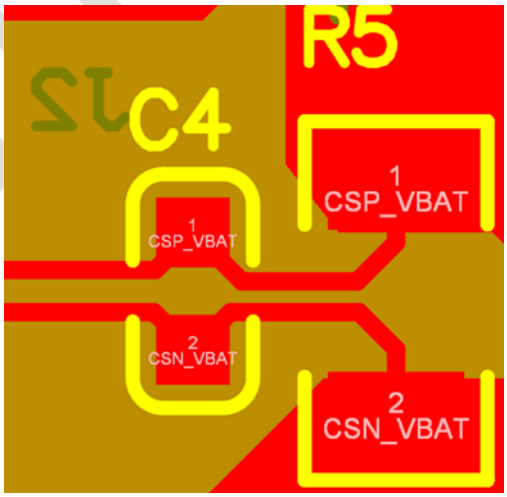


12. PCB Layout Reference

1. Power MOS transistors and inductors, as the main heat generating devices, should be kept away from each other and heat dissipation measures should be taken; Q1~Q4 power MOS transistors are recommended to be placed on the same side of the chip.



2. Kelvin connection should be used to arranging the current sensing traces, pulling them inward from the resistor pad and leading to the CSP_VBAT and CSN_VBAT pins separately, without leading to other places in the route. Similarly, traces on the VBUS side, with a width of 8 mil or 10 mil, should be directly connected to the CSP_VBUS and CSN_VBUS pins through the sensing resistors; the 0.1uF capacitor in parallel with the sensing resistor is placed near the sensing resistor.

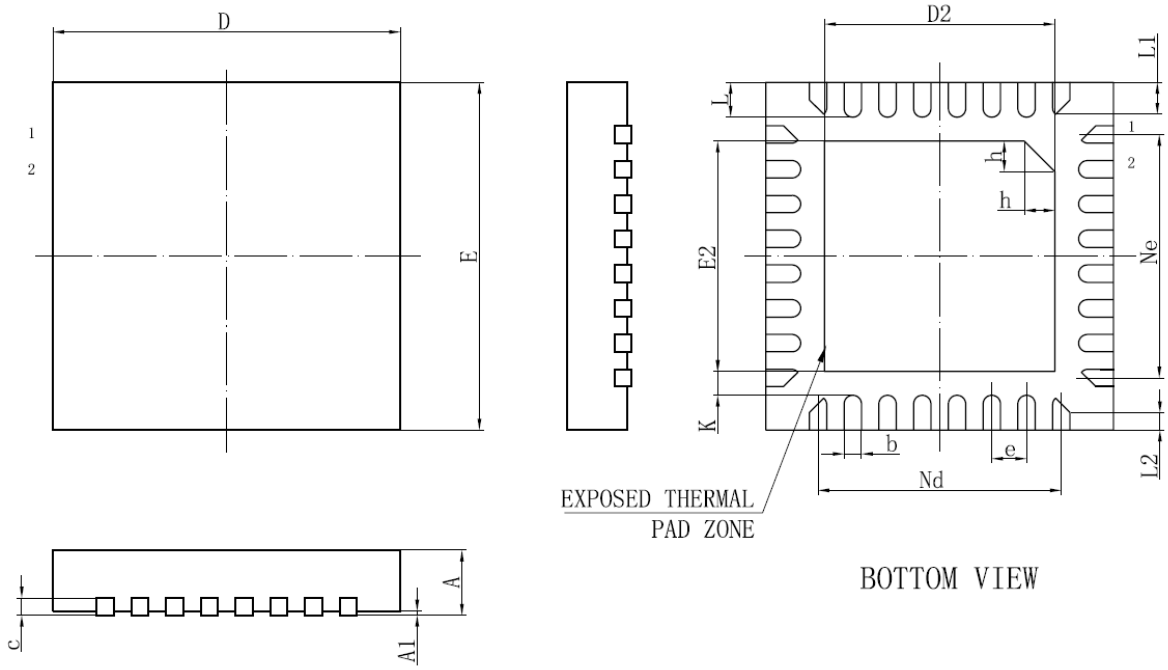


3. General signal traces (not carrying high currents) should have a width of 0.2mm (8mil) or 0.25mm (10mil), and other traces from the chip's HD1, LD1, SW1, HD2, LD2, and SW2 pins to the power components should be at least 0.25mm (10mil) or more in width.

4. Since the high frequency of signal flip at the inductor may affect other signal lines, traces should not be arranged below the bottom of the inductors if possible.
5. The VCC/VDRV capacitors and COMP1/COMP2 compensation networks should be placed near the IC pins.
6. The input capacitors should be as close as possible to the power supply of the power MOS transistors and ground connection, with the shortest possible path;
7. The feedback resistors need to be placed near the FB pins and away from noise sources.
8. The traces of VBUS, SW1, SW2, B+, and GND should be as wide as possible, copper pours are recommended, and the width should not be less than 80mil; the traces of SW should be as short as possible, without change layers. At least 12 vias are needed when high-current network traces change layers. Make as many vias as possible, while considering the integrity of the underlying ground and heat dissipation.
9. The number of vias should be determined based on the size of the overcurrent and the size of the heat dissipation pad when changing layers. More than 12 vias are recommended for VBUS, SW1, SW2,B+ and GND to change layers; more vias are recommended in other spare spaces to strengthen the connection between the bottom layer and the top layer and to facilitate heat dissipation.

13. Mechanical and Packaging

13.1. Package Summary



13.2. Package Outline and Dimensions

Symbol	Dimension in Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40

14. Revision History

V1.0 Initial version.

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